VIRGINIA TECH VTAG ANTENNA GROUP

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A Hybrid DSP and FPGA System for Software Defined Radio

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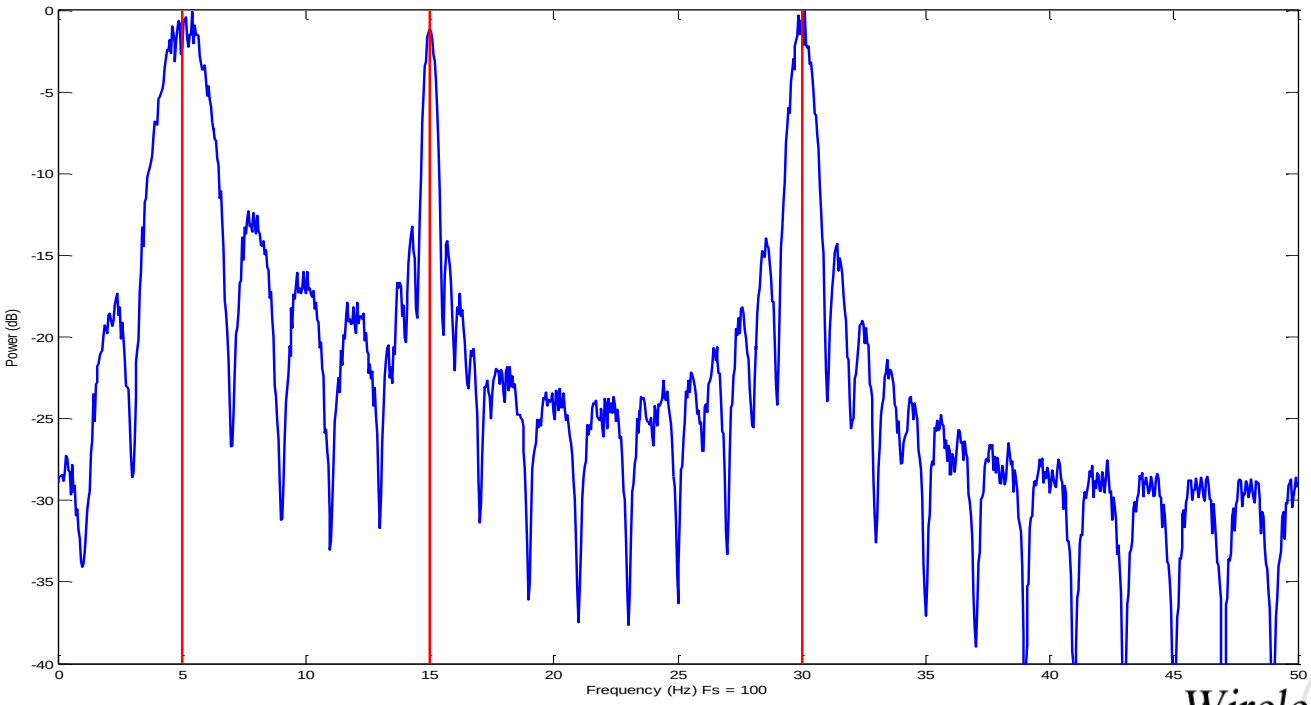
Outline

- Motivation for the project
- Other devices on the market
- Transceiver structure and design
- Testing Results
- Conclusions and Future Work
- Questions

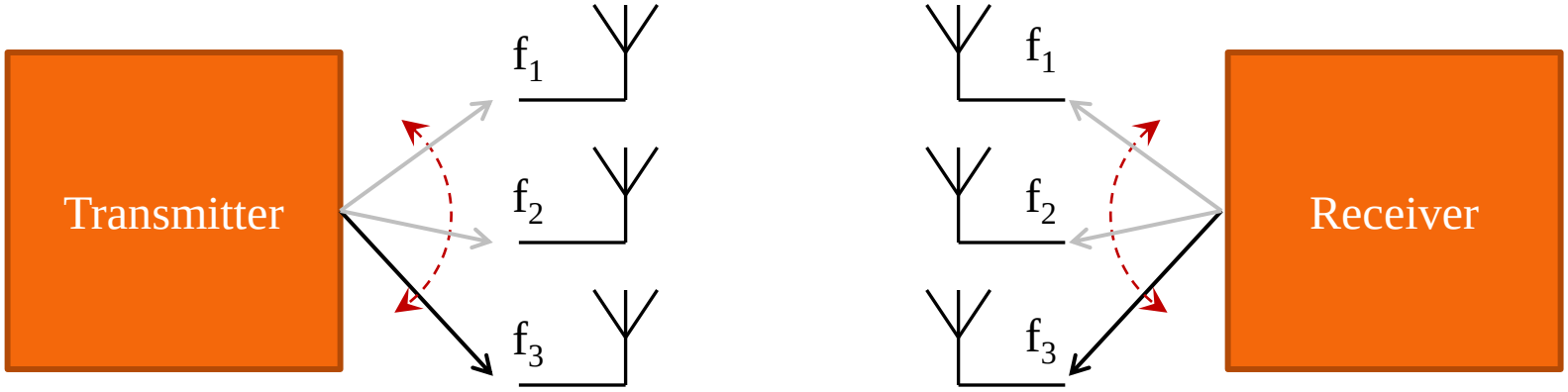
Motivation for the Project

Suppose there are 3 different information channels that need to be received at the same time

- Different bandwidths
- Different modulations



Motivation for the Project



- Instead of wideband antenna, a narrowband antenna with tunable frequency can be used, and hop between frequencies quickly

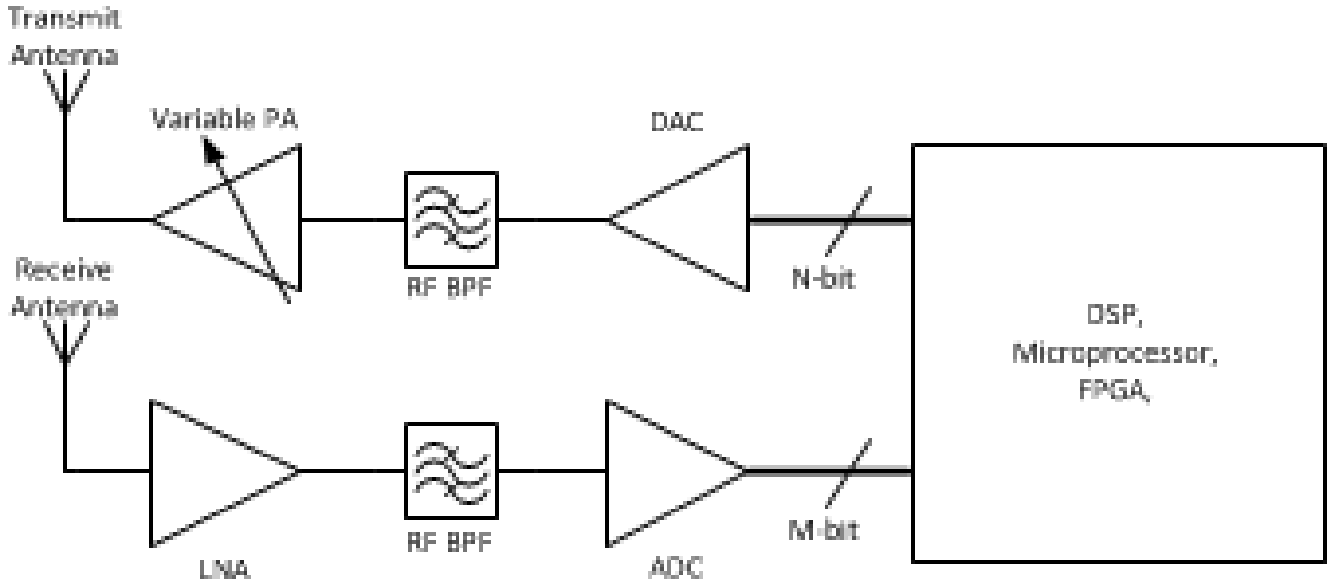
- Need to see if performance drops due to frequency hopping. Need bit error rate (BER) testing platform

Motivation for the Project

- A good way to test system is to use software defined radio (SDR)
  - Can implement any modulation
  - Can modify platform at any time

Why Software Defined Radio?

- Software defined radio is independent of the components, adding a new capability, becomes writing a new firmware, not building a new device.



Software Defined Radio in the Ideal Case

Current SDRs on the Market

Current SDRs on the Market

- There are multiple devices that can be used for Software defined radio on the market

- Ettus Research has 2 platforms, and recently introduced a new one

USRP

USRP2

Current SDRs on the Market

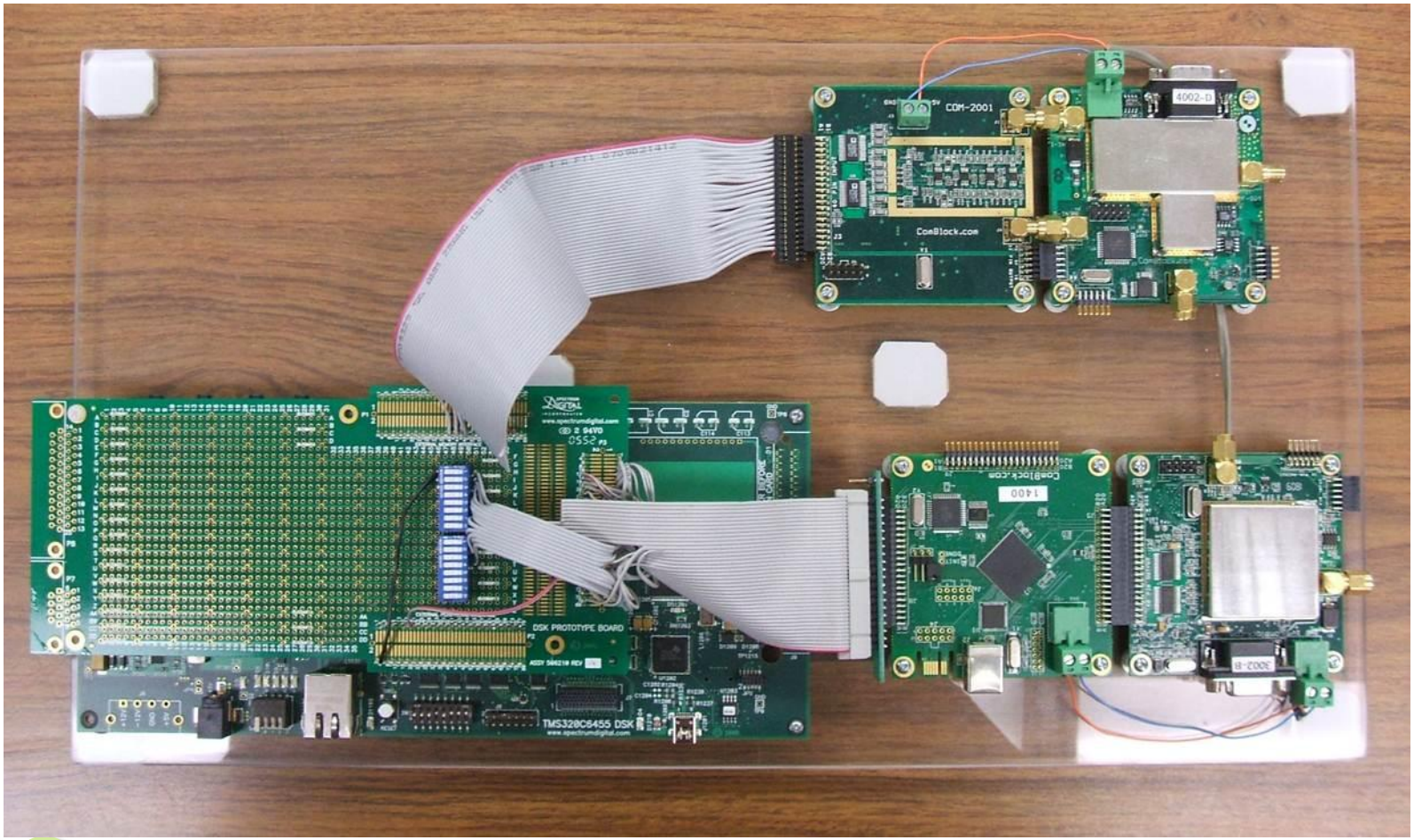
- There is also a Rice University WARP (Wireless Open-Access Research Platform)
- And there is a commercial product from Lyrtech
- ComBlock also has some modules that implement a modem and are developing SDR platform

Current SDR on the Market

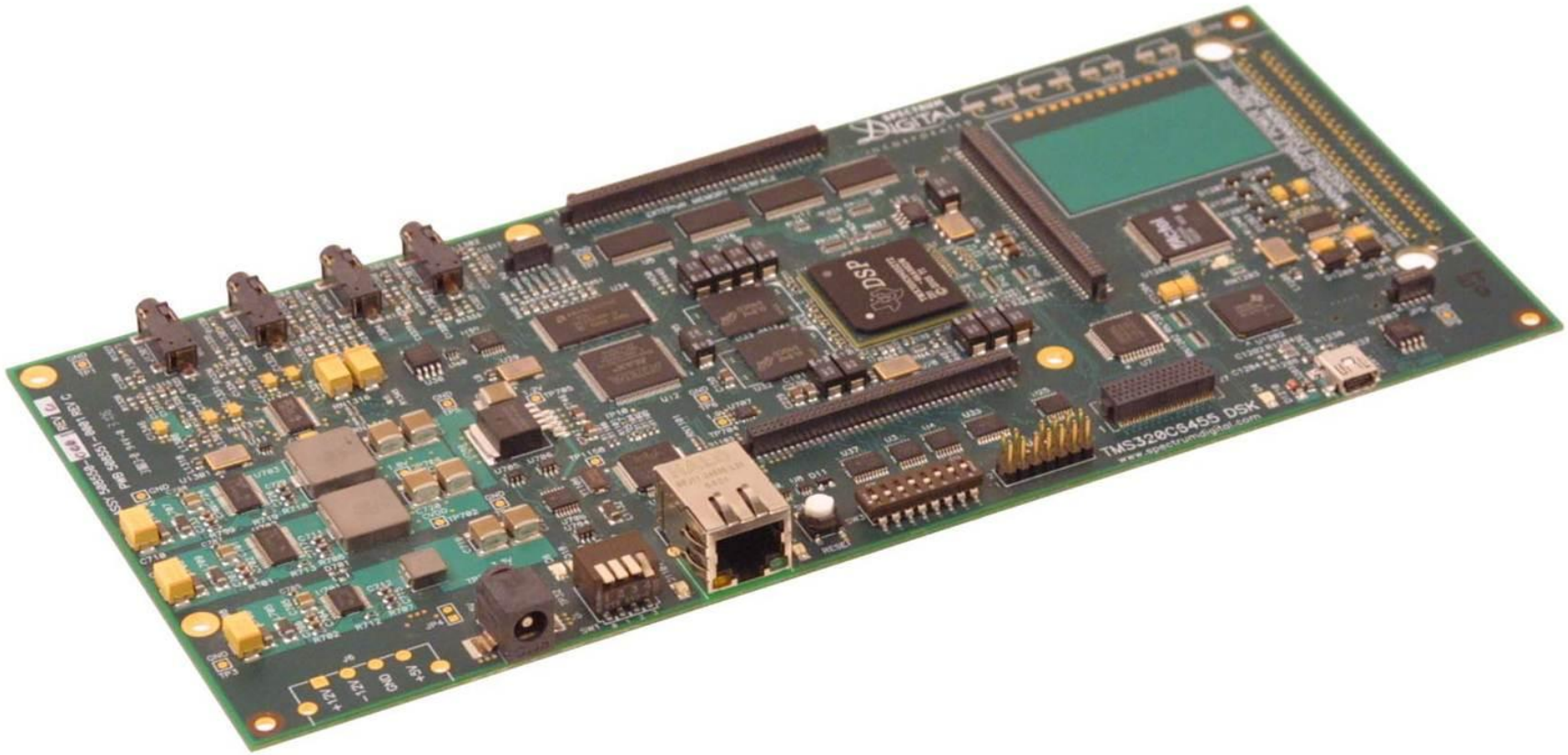
- Rice University WARP platform is pretty expensive, and so are products from Lyrtech
- Ettus Research is a bargain, and there is a large community supporting it with GnuRadio
- ComBlock modules are pre-programmed. Each new feature will require a different block. Or IP (intellectual property) needs to be purchased

Transceiver Structure

Developed SDR platform



TMS320C6455 DSK



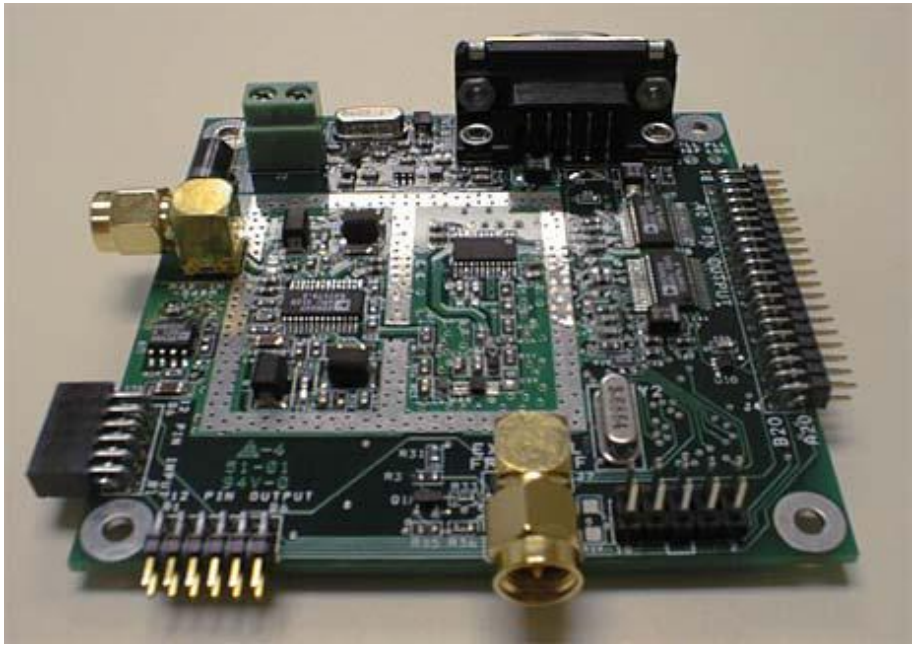
Transmitter

- Transmitter consist of DSP board, a DAC board, and an up-converter modulator
- Modulator range: 950-1450 MHz
- DAC: Max sampling rate 125 MSPS; maximum output bandwidth 13 MHz
- DSP and DAC are connected together using IDE cable through an external memory interface

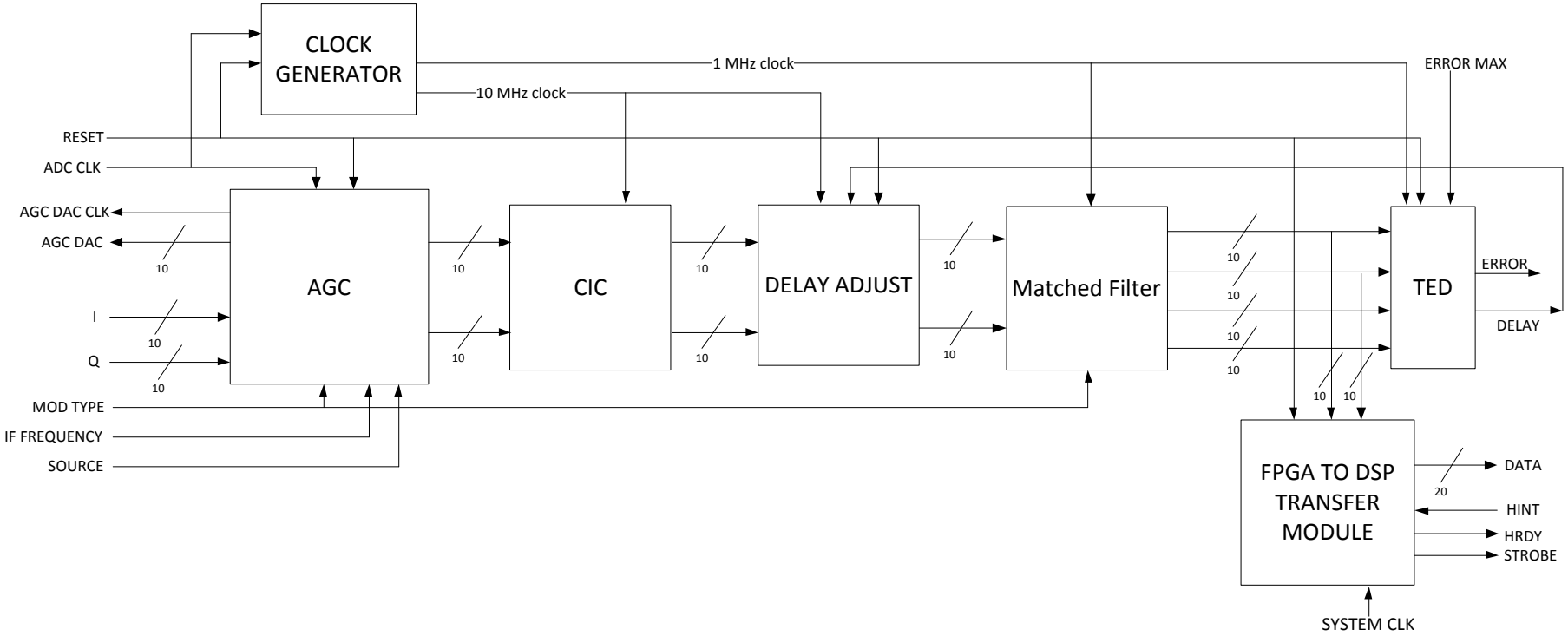
- External interface memory clock is used for the DAC transfers
- At the moment clock rate is 12 MHz

Receiver

- Receiver consists of down-converter demodulator with the ADCs
- FPGA for preprocessing and communication control with the DSP
- Down-converter range: 900-1575 MHz
- ADC sample rate: 40 MSPS



FPGA Block Diagram



FPGA: Xilinx Spartan-3 400

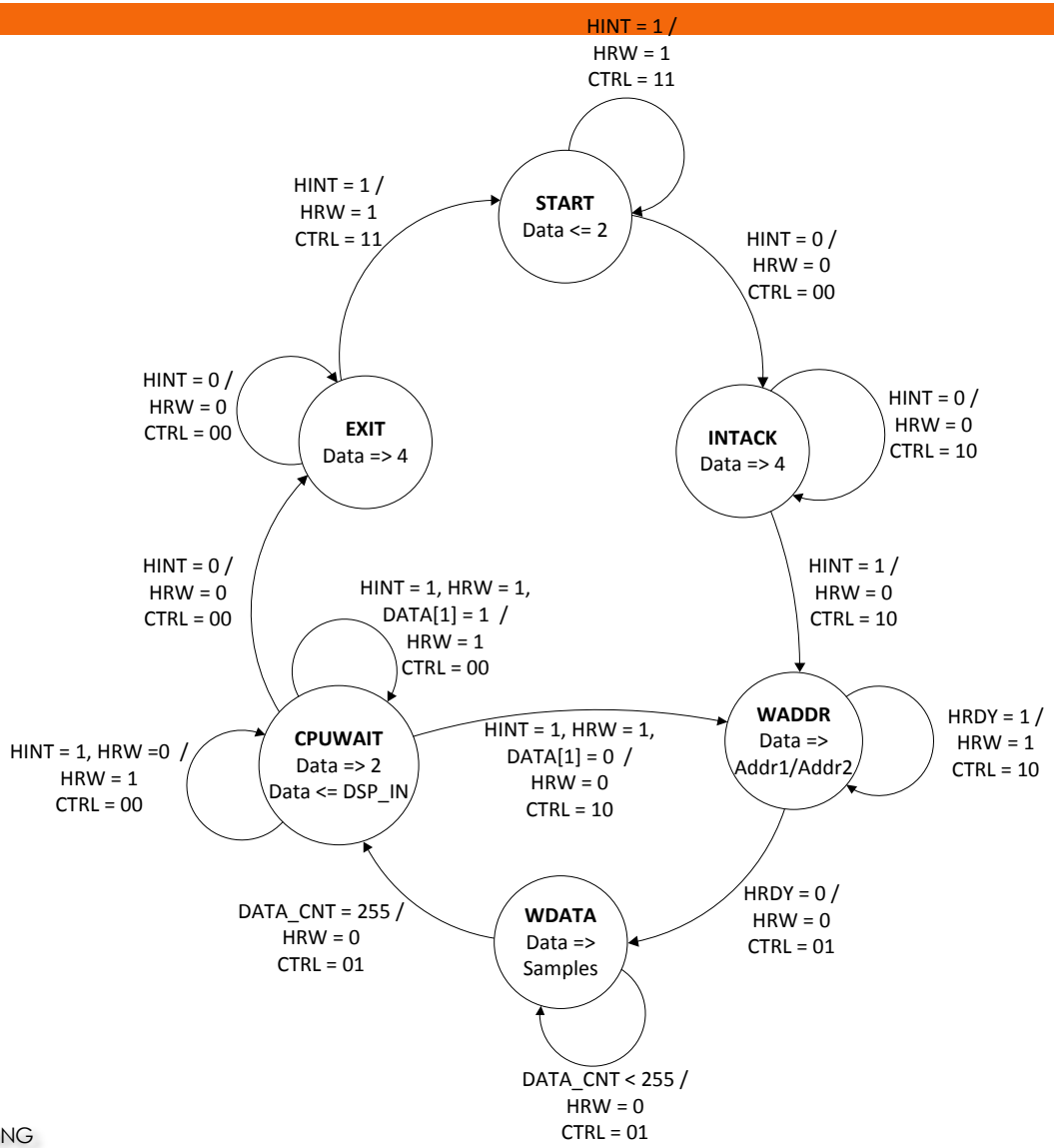
Transceiver Structure

- DSP Code
  - Network Communication
  - Baseband Signal Generation
  - Signal reception and correction
  - Error Calculation

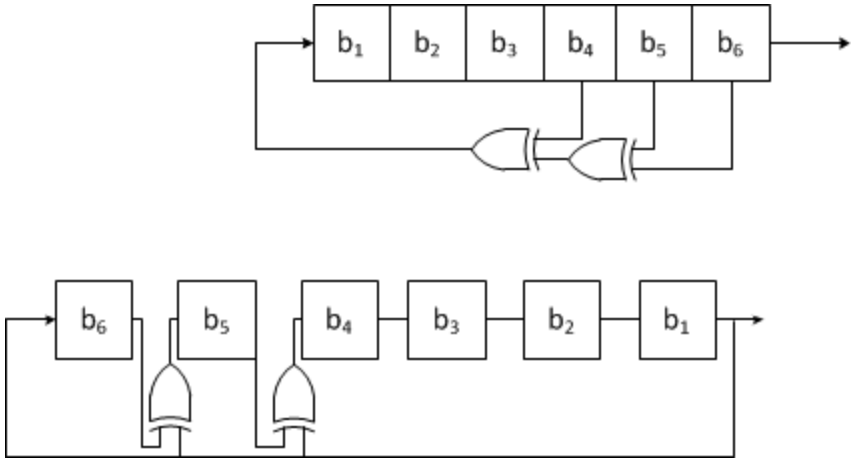
Transceiver Structure

- FPGA Code
  - DC Offset Correction
  - Automatic Gain Control (AGC)
  - IF Down conversion and Decimation
  - Matched Filtering
  - Timing Correction
  - DSP Communication

DSP Communication



Error Generation And Synchronization



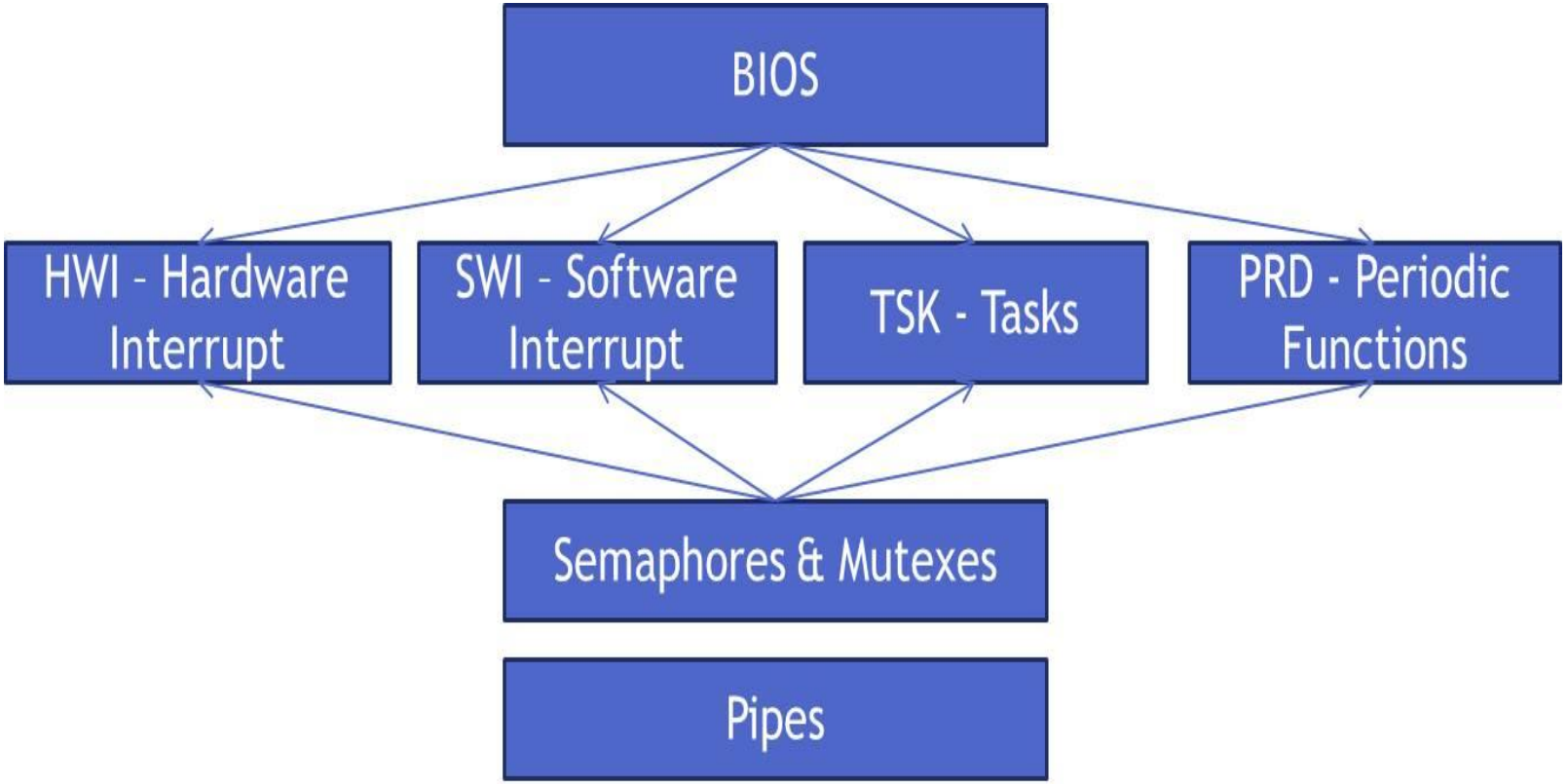
- Linear Feedback Shift Register (LFSR)
- LFSRs are used to generate maximal length sequences (m-sequence)

BIOS

- BIOS is the real-time operating system (RTOS) used in some of the TI's DSPs

- Advantages of the BIOS over traditional coding is the use of scheduler

BIOS Structure



Example of BIOS usefullness

Code without BIOS

```
ISR() {
  Interrupt triggered code
}

main() {
  while(1) {
     Functions();
     Other code;
   }
}
```

Code with BIOS

```
ISR() {
  Call SWI();
}
main()   {
  Call setup functions;
  return;
}
SWI() {
  Process interrupt here;
}
OtherThread() {
  Perform other code;
}
```

Test Results

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Samples of Generated Signals

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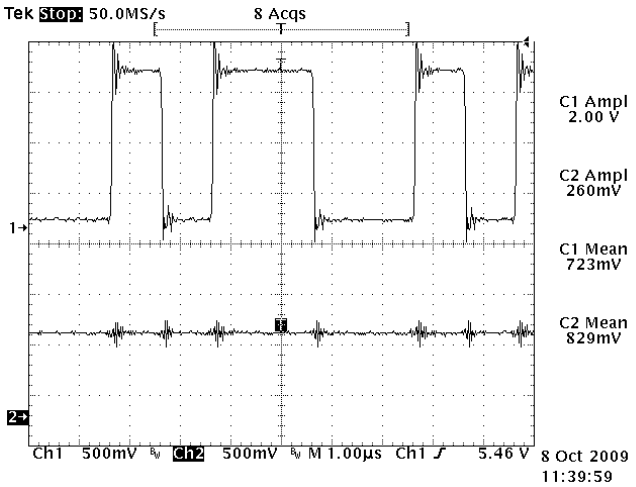

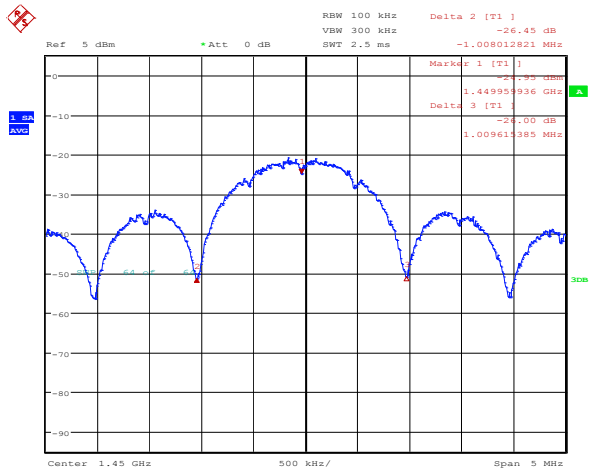

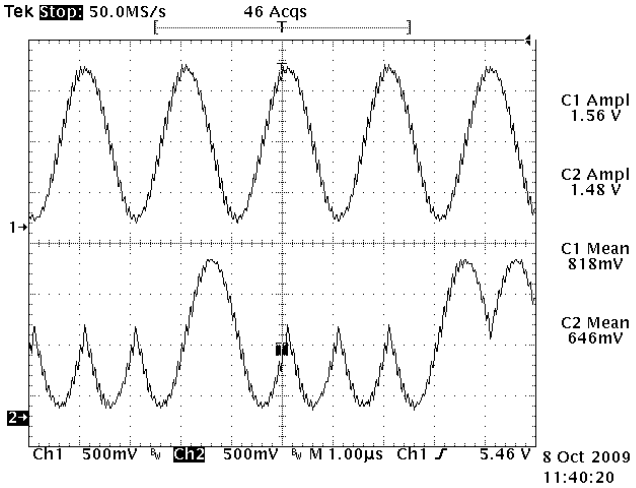

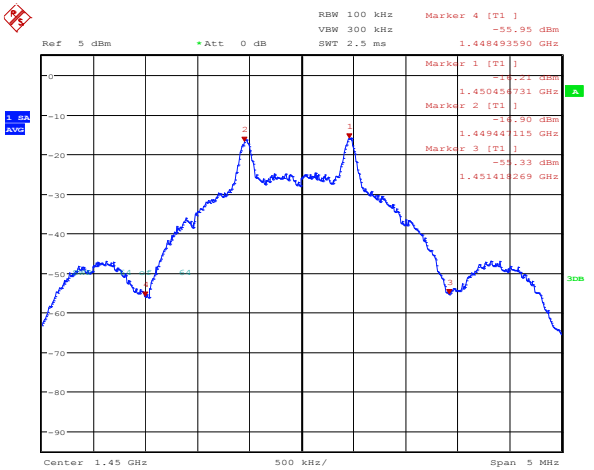

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Samples of Generated Signals

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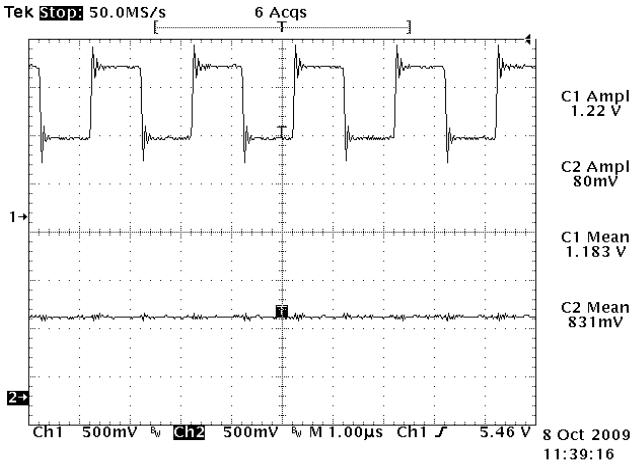

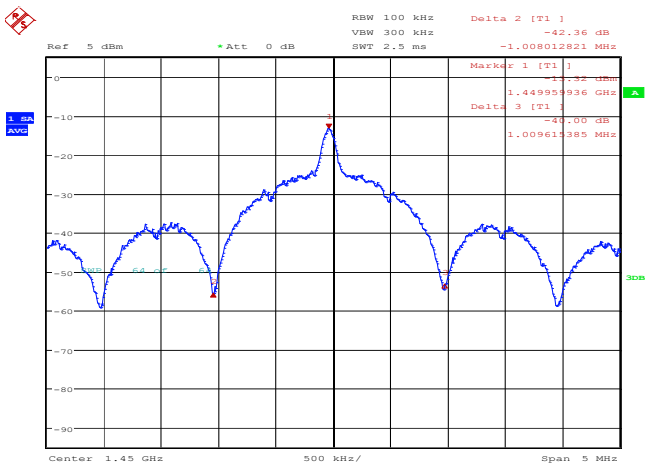

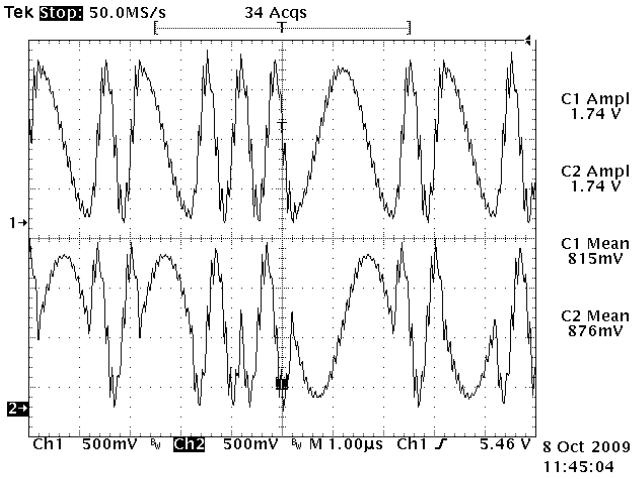

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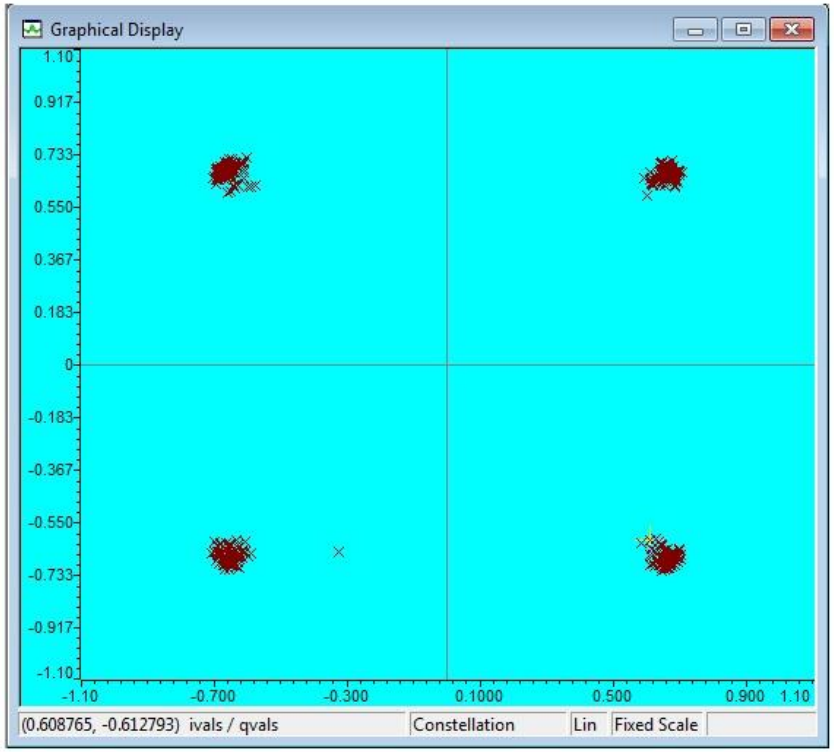
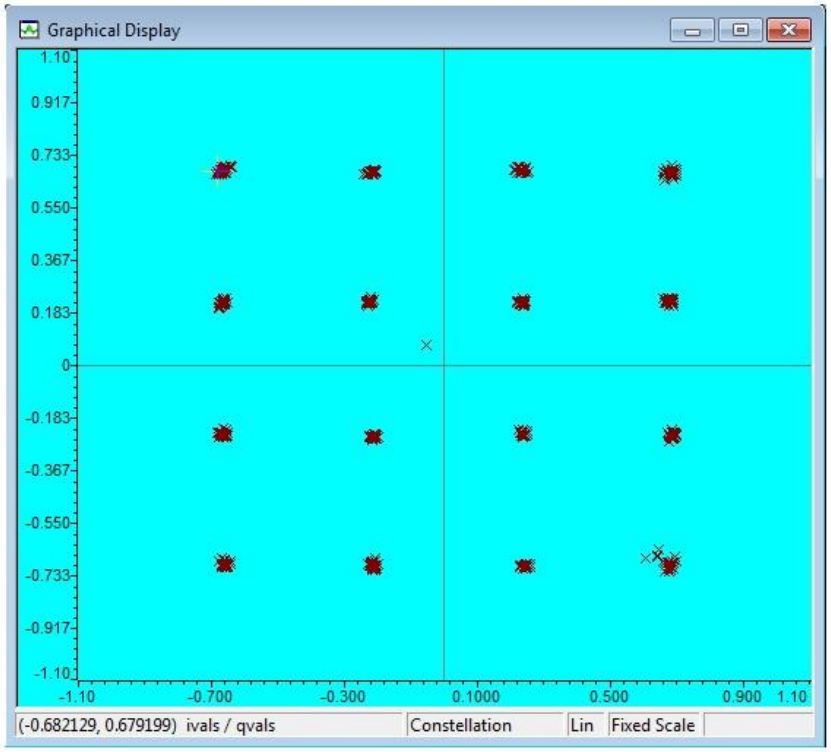
Samples of Demodulated Data

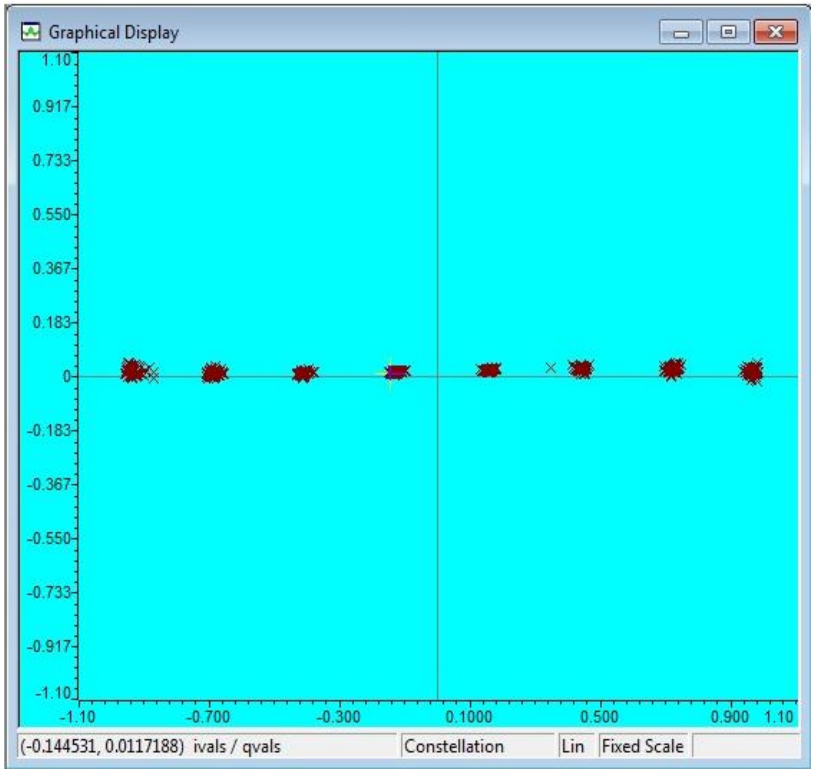


QPSK

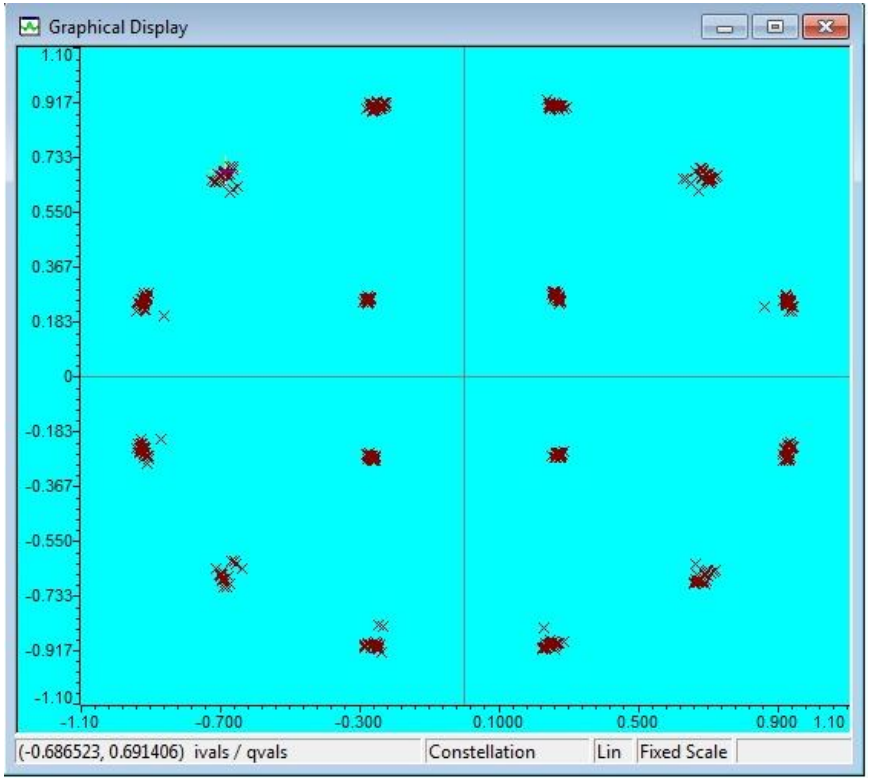


16-QAM

Samples of Demodulated Data

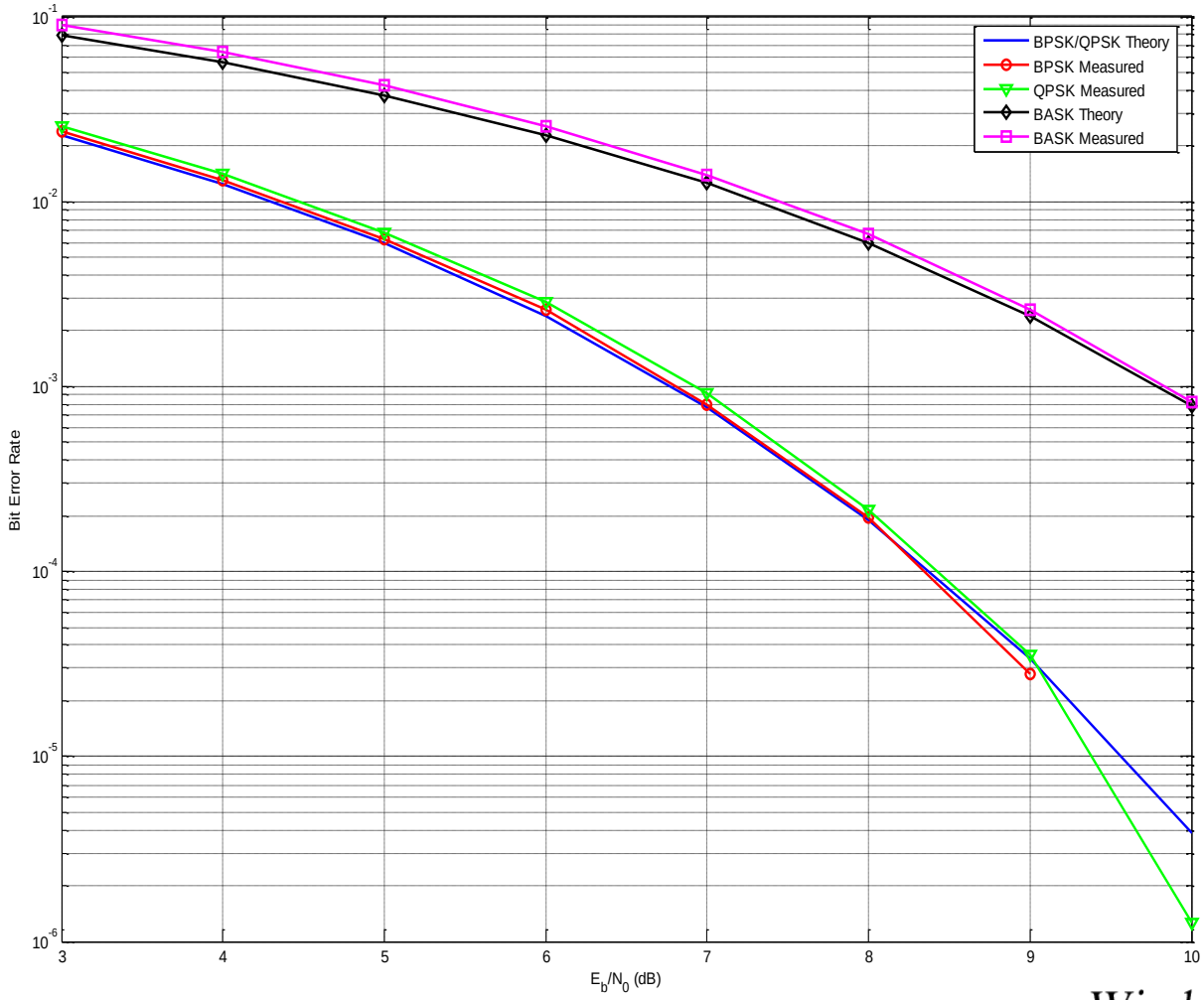


8-PAM

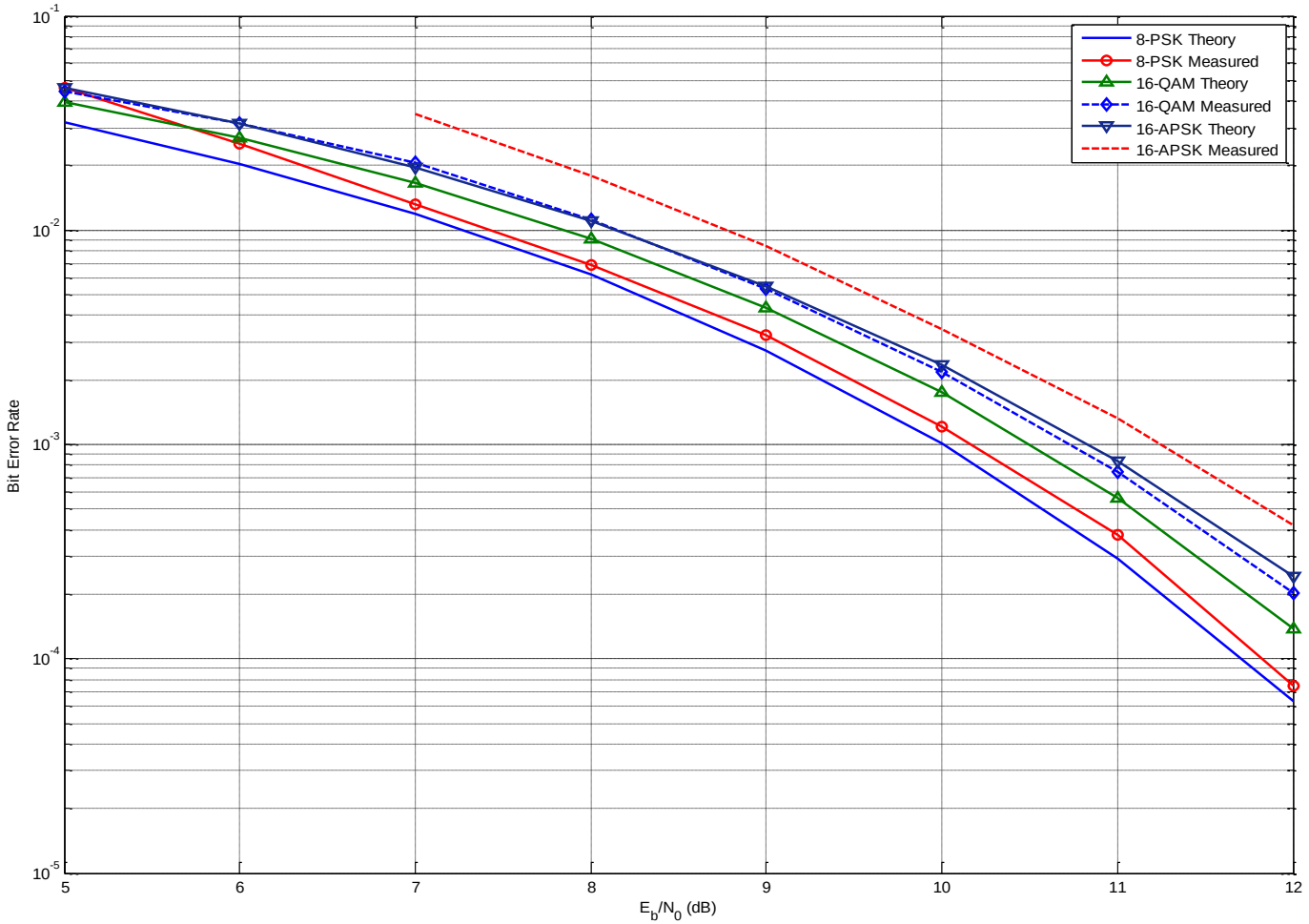


16-APSK

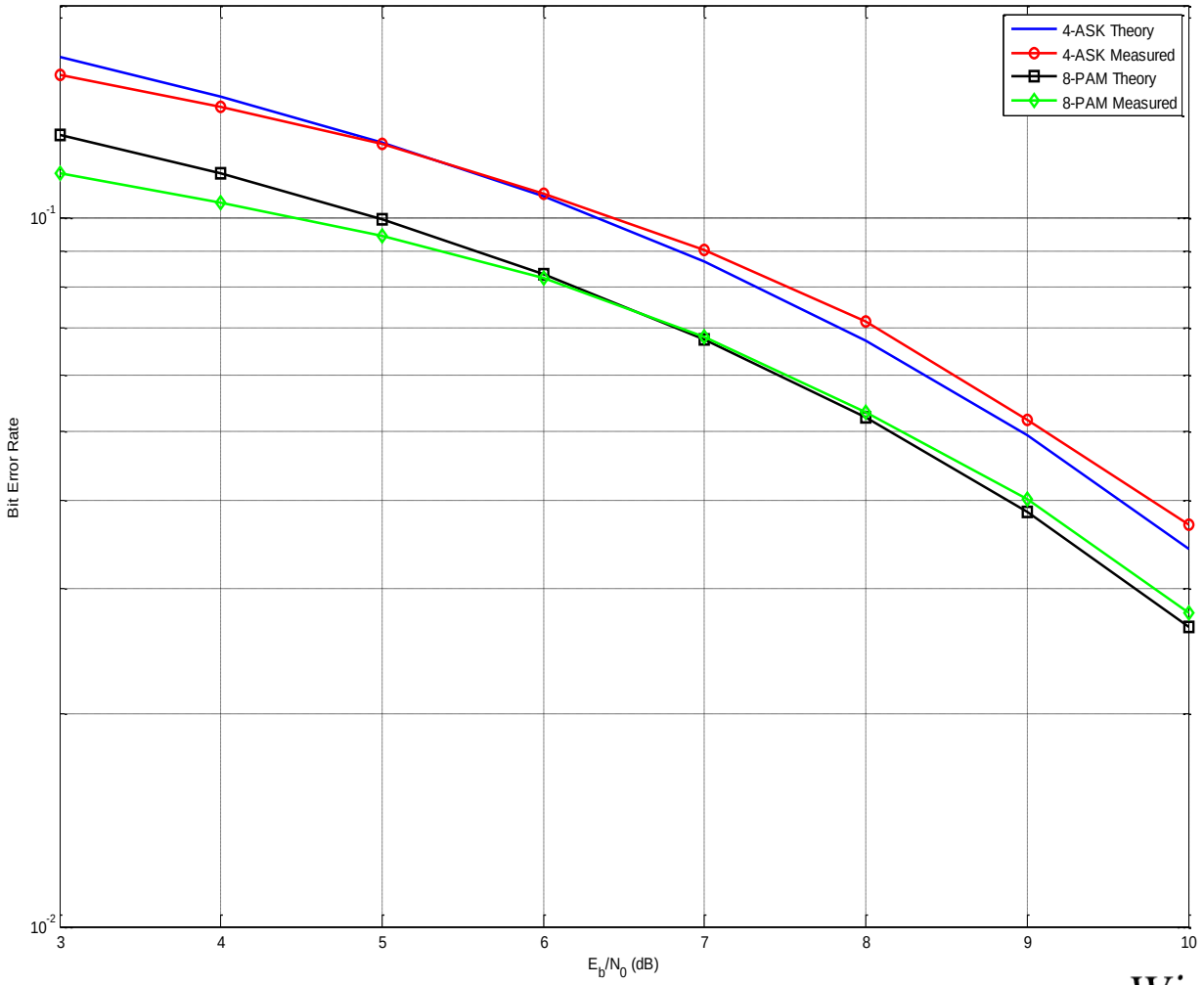
BER Curves


BPSK/QPSK Theory
BPSK Measured
QPSK Measured
BASK Theory
BASK Measured
Bit Error Rate
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
3
4
5
6
7
8
9
10
E_b/N_0 (dB)

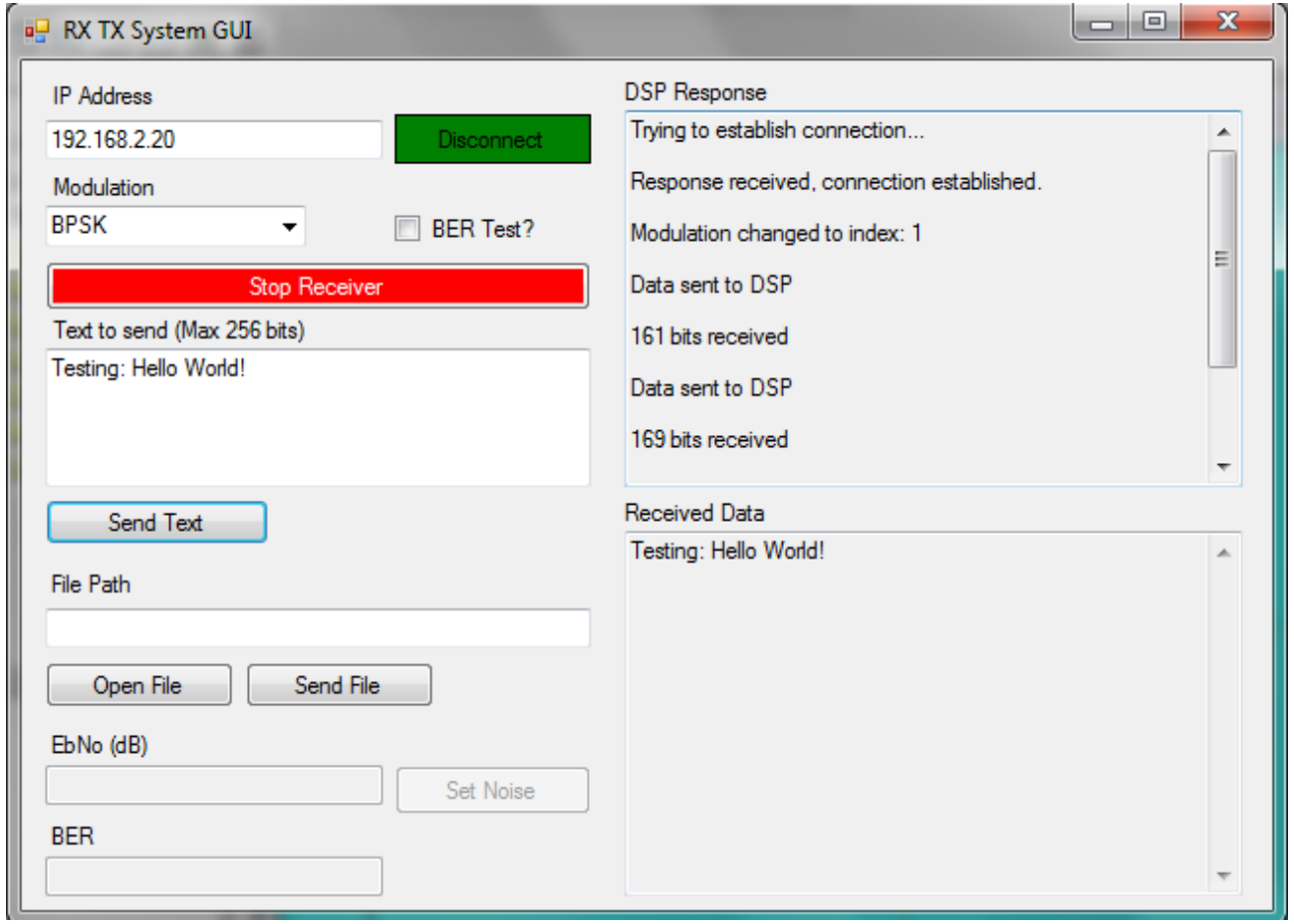
BER Curves


8-PSK Theory
8-PSK Measured
16-QAM Theory
16-QAM Measured
16-APSK Theory
16-APSK Measured
Bit Error Rate
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
5
6
7
8
9
10
11
12
E_b/N_0 (dB)

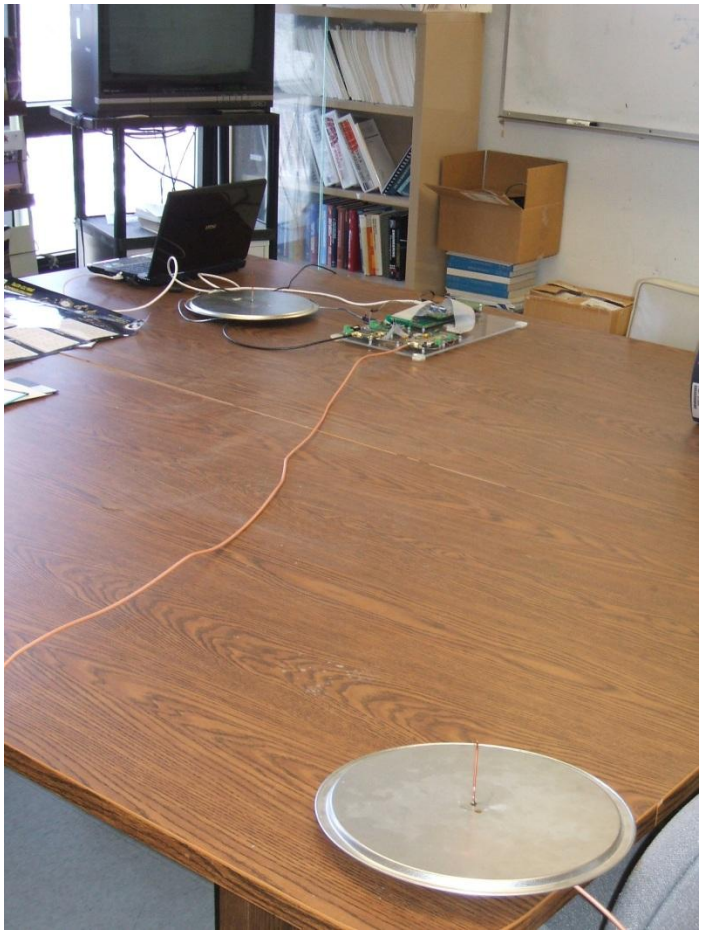
BER Curves


4-ASK Theory
4-ASK Measured
8-PAM Theory
8-PAM Measured
Bit Error Rate
10^{-1}
10^{-2}
3
4
5
6
7
8
9
10
E_b/N_0 (dB)

Network GUI


RX TX System GUI
IP Address
192.168.2.20
Disconnect
Modulation
BPSK
BER Test?
Stop Receiver
Text to send (Max 256 bits)
Testing: Hello World!
Send Text
File Path
Open File
Send File
EbNo (dB)
Set Noise
BER
DSP Response
Trying to establish connection...
Response received, connection established.
Modulation changed to index: 1
Data sent to DSP
161 bits received
Data sent to DSP
169 bits received
Received Data
Testing: Hello World!

Wireless Link Tests



Wireless Link Test Results

Modulation	Error Test 1	Error Test 2
BASK	0.01643164	0.0122165
BPSK	0.0152784	0.01331759
QPSK	0.0072194	0.0188586
4-ASK	0.014609	0.014479
8-PAM	0.032588	0.032715
8-PSK	0.047863	0.0271668
16-QAM	0.0323732	0.024467
16-APSK	0.0248244	0.025308

Wireless Link Test Results

Modulation	Error Test 1	Error Test 2
BASK	0.0165107	0.0164654
BPSK	0.0138805	0.0130997
QPSK	0.021261	0.0235587
4-ASK	0.023284	0.020410
8-PAM	0.0367070	0.03299138
8-PSK	0.030490	0.0347004
16-QAM	0.0252258	0.02521068
16-APSK	0.027396438	0.02745781

Conclusions and Future Work

Performance

- Without timing error, performance of the receiver is very good. Phase ambiguity still should be solved somehow

- Under real conditions there is a 1% - 4% error, which means for reliable link there should be an error coding, but BER will need relative measurements

Future improvements

- Optimizing system for one particular task and modulation
- Peripherals such as audio ADC and DAC can be used to create a full cell phone prototype and test different codecs
- Ethernet can be used to create wired to wireless link
- Based on the industry experience clock crystals on the receiver need to be replaced for quality communication system

Original Concepts

- Use of the TI BIOS system rather then Linux
- A working interface between HPI and an FPGA
- An affordable platform with lots of peripherals and a lot of possible customization
- An educational tool