VRT Radio Transport for SDR Architectures

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DRS TECHNOLOGIES

Agenda

- VITA Radio Transport (VRT) standard for digitized IF
- DRS-SS VRT implementation in SDR RF Tuner
- Pentek VRT implementation in SDR processor
- Notional 8 channel system architecture

Benefits of VRT

Synergy provided by a common Data Framework:

- Within an organization and between organizations
- Common product framework reduces product life-cycle-cost
  - Focuses development of common toolset for demonstration capabilities
  - Improves customer ease-of-use of product upgrade

Open Architecture Framework for SW & HW

- Abstracts interfaces from physical links and HW implementations
- Data structures and SW can be developed independent of HW
- HW can be upgraded with minimal impact on overall architecture
- Scalable and Flexible architectures

Benefits of VRT

Interoperable Data Transport

- **Efficient and flexible data structures** for Sensor Signal data and Meta data
- **Signal Data**
- **Sensor Metadata (Context Data)**
- **Time Stamping**
  - Synchronization of multiple receivers in same/different platforms
  - Coherency between multiple receivers co-located in same platform
- **Multiplexing** of many signal channels onto common link

VRT Protocol Infrastructure

- **Signal Data Packets**
  - Purpose: Convey digitized IF/RF signal data
  - Construct:
    - Packet Identifiers
    - Timestamp
    - Signal Data: 1-32 bits real, complex, floating point, vectors, event flags
    - Trailer

- **Context Packets**
  - Purpose: Convey information on the SDR settings and spatial information
  - Construct:
    - Packet Identifiers
    - Timestamp
    - Context Fields: Freq, BW, Power, Gain, Delays, sampling rate, overload, valid data, event flags

VRT Packet Structure

- Packet Identifier
  - Header
  - Stream ID
  - Class Code
- Time Stamp
- Payload
- Trailer

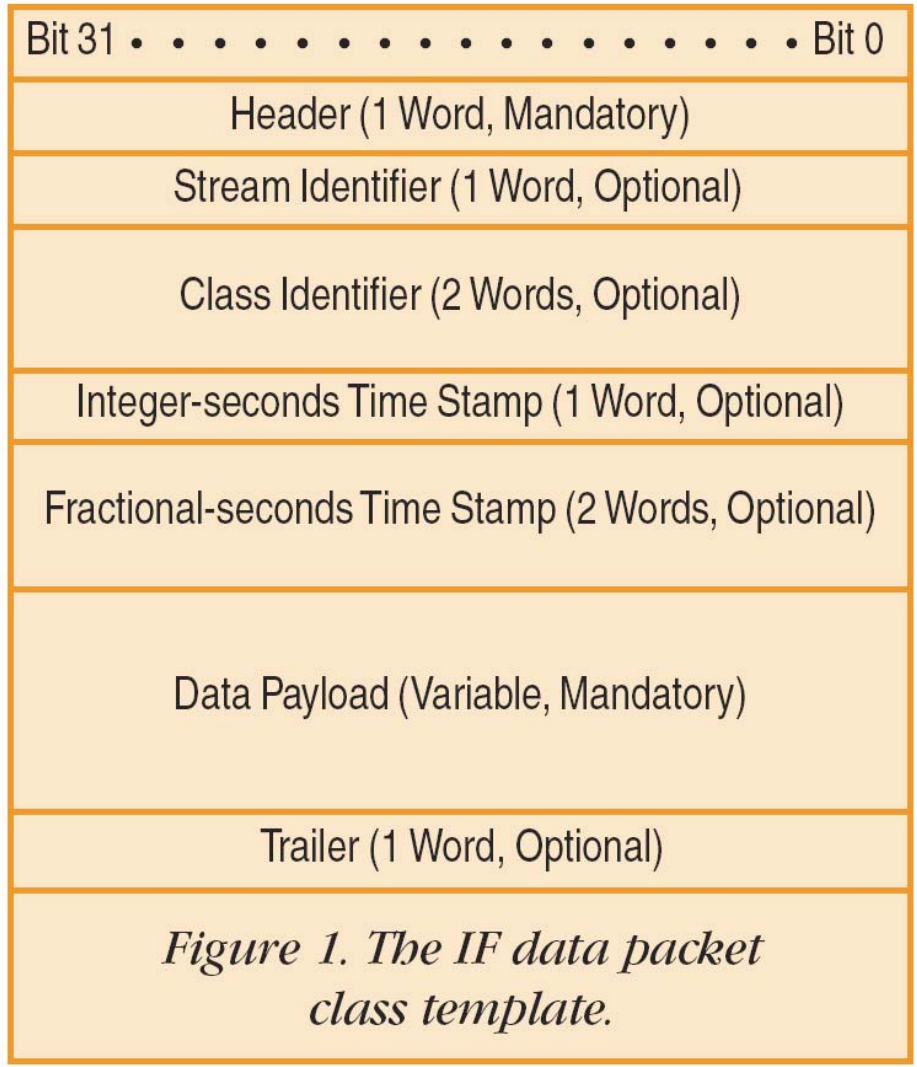


Figure 1. The IF data packet class template.

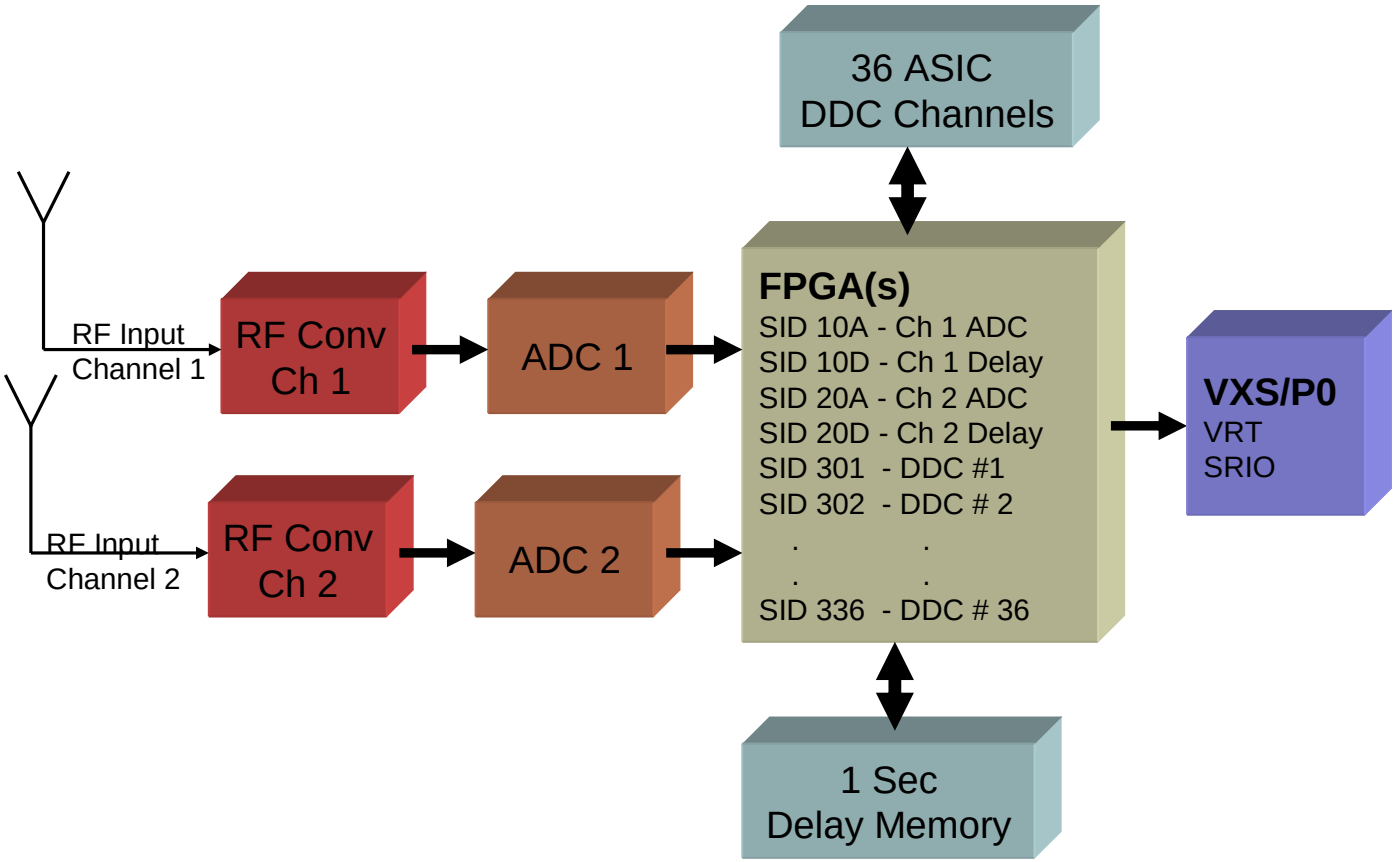
Context Fields

- Context Fields convey a rich set of characteristics
  - Analog settings
  - Digital settings
  - Spatial information
  - Time Delays

Field Name	Min. Range	Max. Range	Resolution
Time Stamp	Present Time	136 years	1 psec or 1 sample
Frequency and BW	–8790 GHz	+8790 GHz	0.95 μHz
Gain or Power	–256 dB or dBm	+256 dB or dBm	1/128 dB or dBm
Sample Rate	0 Hz	+8790 GHz	0.95 μHz

Table 1. Sample of VRT context fields range and resolution.

DRS-SS SI-9147: VXS Tuner SDR



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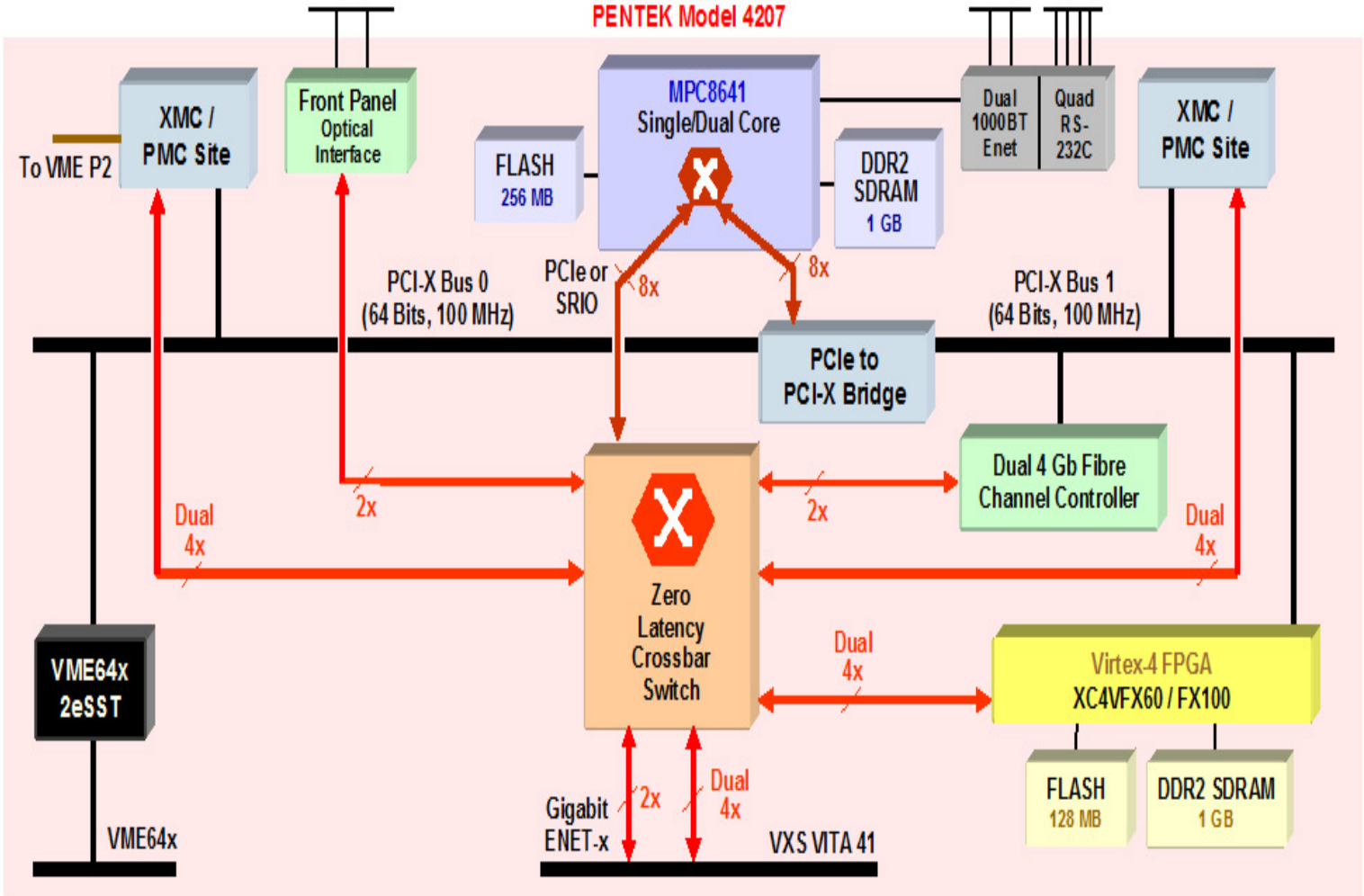
Pentek 4207: VXS Digital SDR



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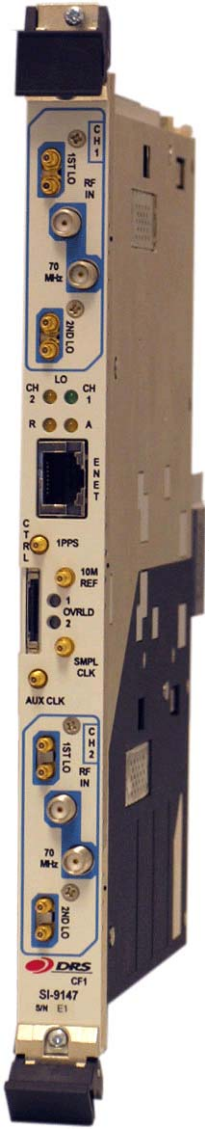
Pentek & DRS VRT Demonstration System



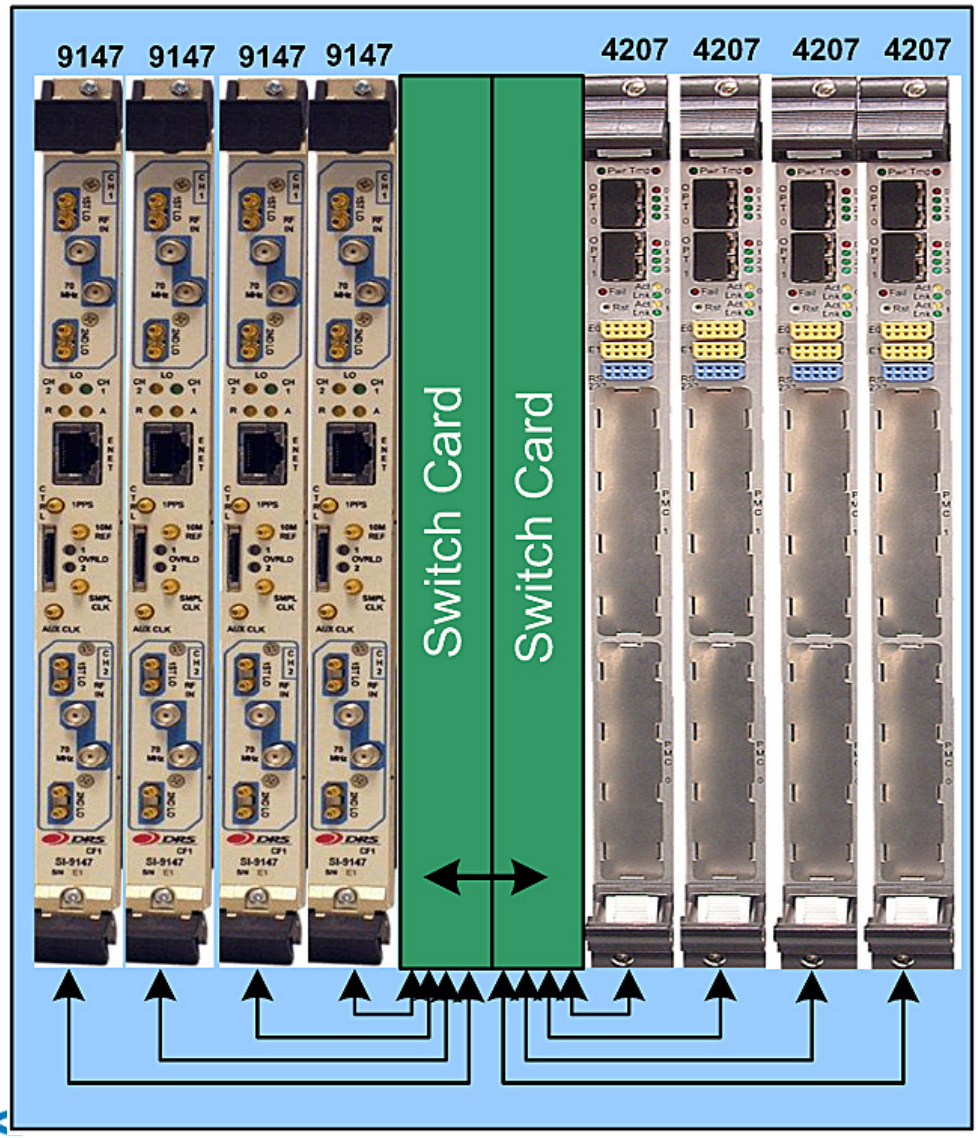
Serial Rapid IO

VRT Packets

DRS-SS SI-9147

Pentek 4207

Eight Channel Multi-Function SDR Architecture



Eight Channel Multi-Function Receiver

- **Dynamic Allocation of Resources**
  - **High speed fabric**
  - **Supports many routing options of signal from antenna to DSP**
  - **Dynamic routing between receiver and DSP components**

- **Simultaneous support of multiple functions**
  - Radar
  - Communications
  - Electronic Warfare
  - Surveillance
  - Other

Conclusion

- **VRT Enhances SDR system architectures**
  - **Eliminates stove-pipe architectures**
  - **Enhances interoperability between components**
  - **Standard for multi-channel phase coherent architectures**
  - **Transport for multi-function SDR architectures**

Appendix

DRS-SS VRT Integration Plans

Product	Form Factor	Digital IF Transport	RF Range	RF Chan	Max Analog BW	DDC	Avail
SI-9136C	VME	**SFPD** **Front panel**	VHF/UHF	2	30 MHz	FPGA	Now
SI-9146	VXS	**P0-Aurora** **P0-SFPDP**	VHF/UHF	2	30 MHz	FPGA	Now
SI-9147	VXS	**P0-SRIO** **P0-SFPDP**	VHF/UHF	2	30 MHz	36 ASIC + FPGA	Now
SI-9149	Brick	**USB 2.0**	VHF/UHF	1	200 KHz	FPGA	Now
SI-9479	Brick	**USB 2.0**	70 MHz	1	200 KHz	FPGA	Now
SI-8728	1U Chassis	**G-E**	HF	8	25 KHz	FPGA options	Q1/2009

VRT independent (agnostic) of physical link
VRT has flexible data structures configurable for sample bit widths and data rates

Pentek VRT Integration Plans

Product	Form Factor	Digital IF Transport	Sample Rate	A/D Chan	Max Signal BW	DDC	Avail
4207	VXS	**SRIO or Aurora**	N/A	N/A	N/A	N/A	Now
6826	VXS	**Aurora**	2 GHz	2 A/D	1 GHz	FPGA	Now
7141	XMC	**Aurora**	125 MHz	2 A/D 2 D/A	50 MHz	ASIC + FPGA	Now
7142	XMC	**Aurora**	125 MHz	4 A/D 1 D/A	50 MHz	FPGA	Now
7151/52	XMC	**Aurora**	200 MHz	4 A/D	80 MHz	FPGA	Now
7156	XMC	**Aurora**	400 MHz	2 A/D 2 D/A	160 MHz	FPGA	Q1/2009

VRT independent (agnostic) of physical link

VRT has flexible data structures configurable for sample bit widths and data rates