TACKLING A SDR PROJECT AS A LAST YEAR PROJECT IN AN ENGINEERING CURRICULUM

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ABSTRACT

Students enrolled in the electrical engineering and computer engineering programs at Université de Sherbrooke have to undertake a mandatory last year design project. Teams of six to eight students work on these projects at a pace of twenty hours per week per student, for a period of eight months (winter and fall semesters). Considering this workforce, design projects of respectable size can be undertaken. We present one such design project that aims at developing an SDR platform that will receive in AM and FM commercial bands while being able to transmit and receive in the FRS band. We explain how this last year design project fits in our engineering curriculum, present the main steps of the project, describe the architecture of the prototype and explain the technical challenges encountered. We also aim at bringing the prototype to the conference for a live demonstration and to report the prototype performance. We hope that this presentation will trigger ideas for other universities to adopt a similar approach for their telecommunication specialty and will be a first step to create an infrastructure within the universities to participate to the SDR Forum Radio Challenge.

1. INTRODUCTION: THE ENGINEERING CURRICULUM AT UNIVERSITÉ DE SHERBROOKE

Université de Sherbrooke is well-known for its coop program that has been established in 1966. With such program, the engineering curriculum is composed of eight semesters plus four work terms of four months each. In this context, engineering students get sixteen months of hands-on experience within industry over a four and a half year period.

Always trying to innovate, Université de Sherbrooke completely changed the way electrical engineering and computer engineering are taught in 2001. Instead of having conventional lectures, an output-based approach is now used where teams of students work on a set of problems associated with a particular theme for a semester. In parallel to this problem-solving approach, students must also complete a semester project for every semester. Combining coop-program and output-based teaching approach, Université de Sherbrooke believes that engineering students will acquire professional and practical skills that will make them very valuable for industry in a short time after graduation.

The fourth year of the curriculum is a particular one: the two last semesters are mostly dedicated to a mandatory last year project, whose scope is much more substantial than for semester projects. In this context, a team of students undertook a SDR project. Following, we present the main project steps, the prototype architecture and the technical challenges encountered.

2. MAIN PROJECT STEPS

In fall 2005, a list of project proposals was presented to the last year students. Project proposals can also be made by the students themselves. Teams of six to eight students were formed based on the students interests for a particular project. There was then some competition among proposals and the SDR project, considering its emerging technology status, had enough traction to get selected. The SDR project team was conveniently balanced with four electrical engineering students and two computer engineering students. Two electrical engineering students were assigned to hardware development, two electrical engineering students were assigned to waveform development while the two computer engineering students have been mandated for the software aspects.

Beginning in January 2006, the SDR project team undertook a project definition effort and had to learn as much as possible about SDR technology. They also concentrated on project planning and produced, in February 2006, a project definition document containing project goal, a preliminary technology analysis and a constraint analysis (time, budget, technology risks, etc.).

The technology analysis has been divided in a hardware part and in a software part. On the hardware side, the team considered an RF board connected to a personal computer (a desktop, laptop or PC-104 embedded computer) via USB. The RF board would bring RF signals to the digital world and vice-versa. Computing would be as much as possible made on the personal computer, although some computing capabilities, either through FPGA and/or DSP processor, could be implemented on the RF board if needed. Down the road, the team became aware of the existence of the Universal Software Radio Peripheral (USRP) platform developed under the GNU radio project [1]. Quickly, this platform was selected as the main hardware platform.

On the software side, the team had to study the JTRS SCA standard [2] and also got strong support from the Communications Research Centre Canada (CRC) about the SCARI tools [3]. It has been decided that the first attempts would be made in a non SCA-compliant way to ensure low-level control of the modulation/demodulation algorithms, of the USRP platform and of the computing platform. In a second attempt, efforts will be made to make the system SCA-compliant using the CRC's SCARI tools.

Overall, the SDR project team spent the first four months conducting detailed project planning and high-level technology assessment. After a coop program work term during summer 2006, the team is back on the project since September 2006. The remaining of the year will be dedicated to project execution, prototype tests and delivery. Most of the work will be completed for the SDR Forum technical conference in November 2006.

3. ARCHITECTURE OF THE PROTOTYPE

The goal of the SDR project is to design a prototype of a radio system that can receive AM and FM commercial bands while being able to transmit and receive in the FRS band. Figure 1 shows the hardware architecture of the prototype.

As can be seen, a total of four RF front-ends are needed to reach the goal. Certainly it could be interesting to do some work toward a universal RF front-end but, given the time and resources available to the team, the four RF front-end solution is the only acceptable one.

Each Rx front-end possesses a similar structure: following the antenna, a low-noise amplifier and a band-specific band-pass filter are used. An input selector is used to select the

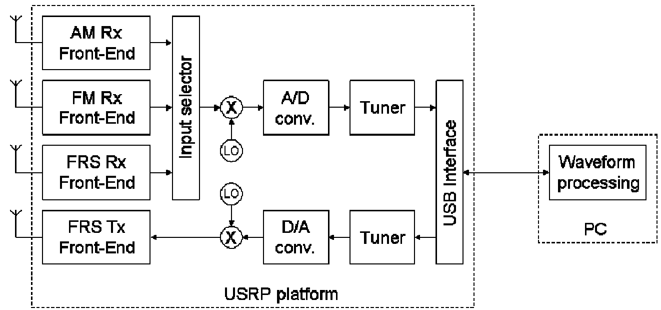

Figure 1 Hardware architecture

targeted frequency band and the transmission or reception function.

A local oscillator is used to translate the selected band to the IF band in the usual way. Care has to be taken so that the signal level from the Rx front-ends is compatible with the dynamic range of the analog to digital converter.

The USRP platform possesses four 12 bits analog to digital converters with 2 V peak-to-peak dynamic range. One of them is used to convert the selected IF signal from the analog domain to the digital domain.

The tuner section, implemented in FPGA, is used to tune the system to a particular operating channel and to provide filtering and down sampling. It generates the I and Q signal components that will be used in the modulation-demodulation process.

As can be seen, two frequency translations of the input signal are performed. The first one, implemented at RF level, selects the desired operation band. The second one, executed via software in the FPGA, selects the frequency operation channel and is a common operation for all the bands and modulations.

The USB interface is used to send the digital signal to the PC for waveform processing.

On the Tx side, the structure is similar, although only one RF front-end is needed.

As can be observed, the A/D D/A converters, the FPGA and the second software mixer form a unique functional platform regardless of the processed signal. This is certainly in accordance with the sought characteristics of SDR systems.

The software side can be divided in the FPGA section and the PC section. Figure 2 shows the FPGA section while Figure 3 shows the PC section.

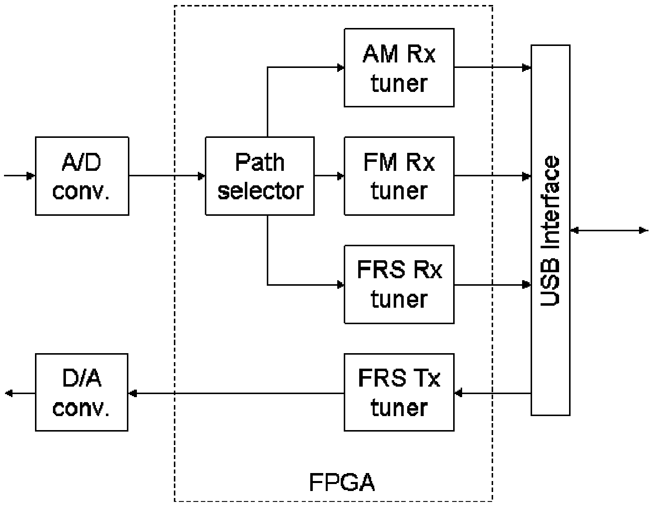

Figure 2 FPGA section

In the FPGA section, the receive path begins with a path selector that distributes the digital signal to the proper Rx tuner. Output of the selected Rx tuner is then transmitted to the PC through the USB interface.

On the transmit path, the FPGA simply implements the FRS Tx tuner. The output signal from the FRS Tx tuner is then fed to the digital to analog converter.

The PC section is running a Linux operating system and the code is written in C++. Depending on the selected waveform, a demodulation selector is used to send the signal of the transmit path to the proper demodulation block. Once demodulated, the baseband signal is played on the PC speakers.

On the transmit direction, the analog signal from the PC microphone is fed to the FRS modulation block. Note that the PC microphone is not the only possible signal source. It is possible to loop back signals from AM/FM/FRS receive paths.

Regarding the modulation and demodulation processes at the PC side, the strategy used in the prototype consists in manipulating adequately the digitized I and Q signals, according to the modulation scheme of the signal. This extends the applicability of the prototype to digital modulation techniques (e.g. QAM). In consequence, the application limitation lies in the analog RF front-end.

4. TECHNICAL CHALLENGES

One of the main challenges of the project is not a technical one but more related to the fact that no one in the team had previous knowledge of SDR radio technology.

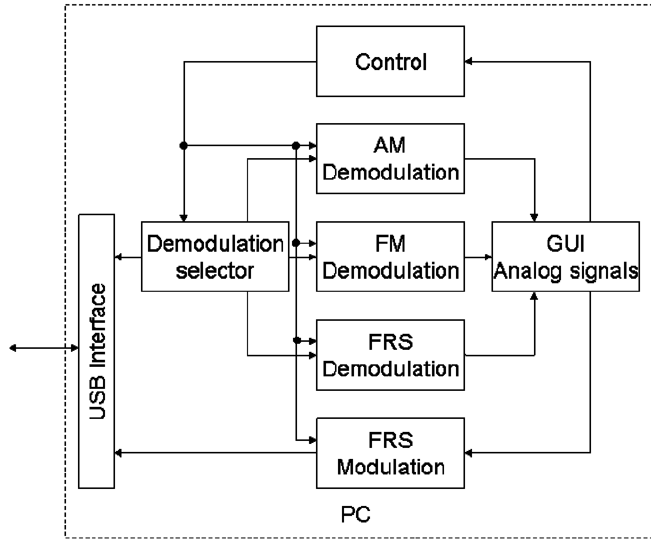

Figure 3 PC section

Consequently, it was difficult for the team, right from the start, to have a clear perception of the amount of work needed to reach the project goal.

At this moment, the goal of the project is much more to produce a functional prototype than to produce a prototype that would include all the qualities of an SDR system. As an example, the software part is absolutely not SCA compliant. Nevertheless, care has been taken to write the software considering a component-based development approach. Consequently, migrating to a SCA compliant version will need minimum adaptation effort.

On the hardware side, it was desirable to use undersampling to minimize analog electronic circuitry. However, the team did not find it appropriate to use this technique with the USRP platform and decided to go forward with an IF stage with analog oscillators.

On the software side, the main challenge was first to get a deep understanding of the whole system. Effectively, libraries provided with the USRP platform require some learning curve. Then, it was necessary to take control of the complete environment. To do so, simple programs that read input samples from the USRP and send them back to the transmit path, without any waveform processing, were written.

As for waveform development, the use of computing software like Matlab was extremely useful. Modulation and demodulation algorithms have been developed and tested in Matlab before being translated to C++.

5. FUTURE PERSPECTIVE

For the remaining of the project, it will be very important to evaluate the performance of the prototype. Then, the prototype will be made SCA-compliant with the help of the CRC SCARI tools. It will also be transferred to a PC-104 form factor embedded computer.

The actual SDR project team members will finish their undergraduate studies in December 2006. Again for 2007, the SDR project will be offered to last year students. Perhaps, building on the work of the 2006 team, the 2007 team might be able to go farther in the sense of building a radio that is closer to the SDR design philosophy: minimizing RF front end circuitry, making signal processing in the digital domain as much as possible and making sure that the system is SCA compliant.

Regarding the possibility to participate to the SDR Forum Radio Challenge, it is our opinion that providing a basic SDR radio system to participating universities will greatly speed up process required to have a student team fully operational and ready to undertake a particular challenge. Also, didactic material, explaining the fundamentals of SDR, would be greatly useful. In our case, students had to find the information by themselves. Without the availability of the USRP platform, it would not have been possible for our team to build a prototype like the actual one in the available timeframe.

6. ACKNOWLEDGMENT

The authors acknowledge the contribution of Konin Calliste Koua, Ahmed Cherkaoui and Mirna Yazmin Castaneda Hernandez that joined the SDR project team for the last four months.

10. REFERENCES

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