IMPLEMENTATION OF A DIGITAL IF TRANSCEIVER FOR SDR-BASED WIMAX BASE STATION

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ABSTRACT

This paper presents the implementation and performance of a Software Defined Radio (SDR) technology-based-Digital Intermediate Frequency (IF) transceiver for IEEE 802.16d standard, often referred to as a WiMAX (Worldwide Interoperability for Microwave Access) base station. The implemented Digital IF transceiver is reconfigurable to three bandwidth profiles : 1.75MHz, 3.5MHz, and 7MHz each incorporating the IEEE 802.16d WiMAX standard. This transceiver can be reconfigured to other WiMAX profiles through software downloaded onto identical hardware platforms, without changing any components or parts on board. Experimental results are presented that show the performance of the designed Digital IF transceiver using an undersampling scheme, which is closely related to the sampling clock jitter characteristics. The experimental results show that the Error Vector Magnitude (EVM) value of the downlink IF output signal for Clock I, with a phase noise of -91.1 dBc/Hz decreased by 13.7 dB more than that of Clock III, with a phase noise of -118 dBc/Hz, the result being unrelated to the WiMAX profile that was operating.

1. INTRODUCTION

Software Defined Radio (SDR) technology is a promising feature for next-generation mobile communication systems. The commercialization of this technology currently centers on the core technologies, such as high speed Analog to Digital Conversion / Digital to Analog Conversion (ADC/DAC) technologies of base station systems. Moreover, the Digital Signal Processing (DSP) processors associated with SDR are rapidly evolving. For example, ETRI(Electronics and Telecommunications Research Institute) is developing a double-mode base station termed a Reconfigurable Base Station (RBS), which is reconfigurable to an IEEE 802.16d WiMAX system based on Orthogonal Frequency Division Multiplexing (OFDM) technology and to a HSDPA (High Speed Downlink Packet Access) system based on CDMA (Code Division Multiple Access) technology. An RBS uses SDR technologies in which modems and other functional blocks can be reconfigured easily, with software downloaded onto identical hardware platforms.

Worldwide Interoperability for Microwave Access (WiMAX) is a fixed broadband wireless access system technology termed IEEE 802.16d MAN (Metropolitan Area Network) technology which has wider coverage compared to 802.11 series standards[1]. Currently, the standardization of IEEE 802.16e is underway, and this standard promises to support enhanced mobility and coverage. The WiMAX Forum, a worldwide industry consortium worldwide, is leading and supporting all these activities to spread this technology, including equipment and services. Field trial tests are being conducted by many companies and manufacturers, which are also preparing commercial services all over the world.

The RBS based on SDR technology adopted the open hardware platform architecture of Advanced Telecom Computer Architecture (ATCA). All the functional hardware blocks and components of the RBS, including the implemented transceiver board, termed ADCB (Analog Digital Conversion Block), follow the ATCA architecture. The ADCB board manages the Digital Intermediate Frequency (IF) function in the RBS, which incorporates heterodyne architecture.

Software radio architectures can be identified where the analog to digital conversion takes place in view of translating an RF analog signal to digital signal. As analog to digital conversion takes place near the receiving antennas, it is evident that software architecture can achieve increasing flexibility via increased programmability[2]. As SDR technology based base stations become commercially available, Digital IF technology will play an increasingly important role in implementing the base station transceivers[3][4][5]. Digital IF technologies incorporate solutions to problems that easily occur on conventional heterodyne systems using analog components such as rejection of Inphase / Quadphase signal mismatch and DC offset problems. Therefore, Digital IF transceivers can provide higher performance than analog IF transceivers having signal distortion by nonlinearity, because they can combine

multiple Frequency Assignments (FAs) on a digital domain using the complex quadrature modulation and demodulation technique for a multicarrier system. The ADCB board incorporates Digital IF technologies and can be reconfigured to other access mobile standards through a Field Programmable Gate Array (FPGA) program and processor software downloaded onto identical hardware platforms.

The main functions of Digital IF transciever include the frequency upconversion of a baseband signal from a modem operating on a Baseband Processing Block (BPB) board to an analog IF signal in addition to the frequency downconversion of an analog IF signal from an RF transceiver to a digital baseband signal. The RF transceiver downconverts the RF signal from a receiver-antenna to an analog IF signal. In addition, the Digital IF transceiver has a channelization function that splits one Analog to Digital Converter (ADC) output signal into two paths for two FA signal-processing events on the downconversion side, and combines the two FA digital signals into one combined digital signal. The one combined digital signal is then entered into the Digital to analog converter (DAC) on upconversion side, as the RBS supports two FA diversity paths in both the uplink and downlink directions.

This paper is organized as follows. In section 2, the overall Digital IF transceiver architecture and design specifications, including an implemented printed circuit board (PCB) assembly module, are presented. In section 3, a reconfiguration function to the three WiMAX profiles through a software download is verified by examining the frequency response spectrum and constellation of the downlink IF transceiver output signal. Furthermore, experimental results are presented that show the performance of the designed Digital IF transceiver using an undersampling scheme, which is closely related to sampling clock jitter characteristics[6]. Finally, concluding remarks are presented in Section 4.

2. IMPLEMENTATION OF DIGITAL IF TRANSCEIVER

In this section, we introduce the overall Digital IF transceiver architecture and design specifications, including an implemented PCB assembly module.

Generally, in view of Digital IF transceiver, DAC data sample rate must be considered in selecting IF frequency. In addition, digital images would not be overlapped each other after ADC when using an in-band alias. Because the adopted DAC can operate at a conversion rate of 400 Msps, theoretically, we can boost the IF frequency up to 100MHz by Nyquist sampling criteria. In the RBS we selected the IF frequency as 80MHz, and the ADC sampling frequency as 64MHz, i.e., interpolated by 8 with a fundamental frequency of 7 MHz * 8/7 = 8 MHz incorporate with WiMAX 7 MHz profile. The adopted ADC satisfies a 64MHz sampling clock rate, because it has a maximum 80Msps sampling rate.

The transmitter side architecture of the presented Digital IF transceiver for a 7 MHz profile WiMAX base station supporting 2 FAs is shown in Fig. 1. It takes a functional block for frequency upconversion and digital combining of 2 FA signals for the downlink direction. Digital IQ baseband signals received from a modem corresponding to each FA are sent to the Digital IF transmitter at a rate of 2 oversamples of the fundamental frequency of the WiMAX system. These digital data are transmitted by the serial Multi gigabit Transceiver (MGT) differential line through a backplane.

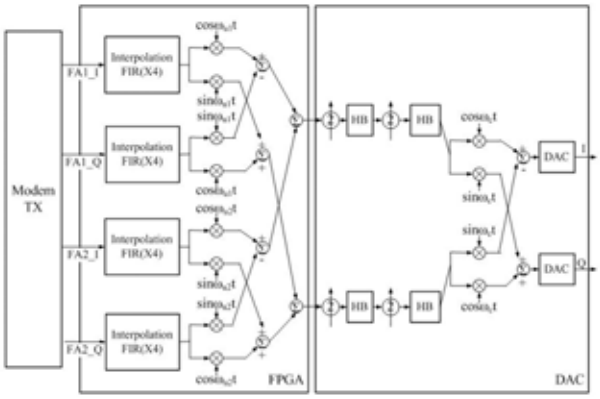

Figure 1. Architecture of ADCB transmitter for a WiMAX 7 MHz profile.

Each digital signal is interpolated to a higher sample rate signal by passing through the x4 interpolation Finite Impulse Response (FIR) filters. As can be seen in Fig. 1 each signal is a digital complex quadrature modulated to a higher frequency using a numerically controlled oscillator (NCO) to remove the image signals. After this modulation, the 2 FA signals are digitally combined to each Inphase and Quadphase signal entering the commercial DAC chip. Here, ω_{u1} = 12 MHz, ω_{u2} = 20 MHz and ω_c = 64 MHz. The DAC is operating at a data rate of 64MHz and uses the two halfband filters to achieve x4 interpolation function internally. Finally, it outputs an IF analog signal of 80 MHz after being upconverted by 64 MHz via digital complex quadrature modulation.

The designed digital FIR filter specifications are shown in Table 1, according to three WiMAX profiles. Because signal bandwidths and digital sample rates differ for each of the WiMAX profiles, the filters should be designed individually. All interpolation filters have the

same type of raised cosine filter and the same number of tabs, specifically, 129. We focused on FIR performance and speed rather than logic cell dimensions when we designed the digital filters, because, as the cost of semiconductor is decreasing rapidly nowadays, it is not important to save the logic cell number. We also used the same filter on the downconversion side for the receiver.

Table 1. FIR filter specifications

Profile	7MHz	3.5MHz	1.75MHz
FIR type	Raised cosine	Raised cosine	Raised cosine
Interpolation rate	x 4	x 8	x 16
Rolloff factor	0.115	0.115	0.115/ 0.115
Number of Taps	129	129	129/129
Sampling frequency(MHz)	64	64	64/8
Cutoff frequency(MHz)	3.5	2	2/1.2
Coefficient width(bits)	16	16	16/16

Table 2 shows main transmitter specifications of ADCB for downlink direction.

Table 2. Transmitter specifications for downlink

Profile	7MHz	3.5MHz	1.75MHz
IF output frequency	80MHz		
IF output power	-13dBm ± 3dB		
IF output signal bandwidth (MHz)	7	3.5	1.75
Number of FA	2		
Center frequency of FA (MHz)	FA1 : 76MHz FA2 : 84MHz		
Baseband signal from Modem	64MHz LVDS		
DAC bit resolution	16		
DAC sample rate	256MHz		
Impedance	50 ohm		

Figure 2 shows the architecture of the ADCB receiver side for the uplink direction. The receiver side has two main functions, frequency downconversion and channelization, that split one ADC output signal into two paths. The input of this receiver is an analog IF signal from an RF transceiver. Here, the RF transceiver downconverts the RF signal from a receiver antenna to an analog IF signal. This analog IF signal to Digital IF receiver side involves analog to digital conversion through an ADC operating with a 64 MHz sampling clock rate. This signal is then split into two paths for FA channel splitting. After being demodulated to the baseband signal using the NCO blocks, the output signal is downsampled by 4 through a decimation filter adapted to each I and Q path. Here, ω_{d1} = 12MHz, and ω_{d2} = 20MHz in Fig. 2.

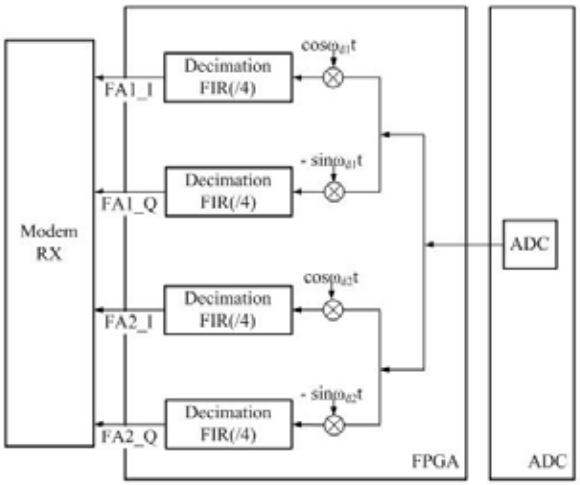

Figure 2. Architecture of ADCB receiver for a WiMAX 7 MHz profile.

Table 3 shows the main receiver specifications of the ADCB for the uplink direction.

Table 3. Receiver specifications for uplink

Profile	7MHz	3.5MHz	1.75MHz
IF input frequency	80MHz		
IF input power	-10dBm ± 3dB		
IF input signal bandwidth(MHz)	7	3.5	1.75
Number of FA	2		
Center frequency of each FA(MHz)	FA1 : 76MHz FA2 : 84MHz		
Baseband signal to Modem	64MHz LVDS		
ADC bit resolution	14		
ADC sampling rate	64MHz		
Impedance	50 ohm		

Figure 3 shows a Digital Processing Sub-system (DPS) rack, which manages external network interfaces and the digital signal processing function of RBS system. In this figure, the board marked with a dotted red line is the ADCB board of the Digital IF transceiver. This board can adopt two Digital IF conversion Modules (DICMs) to support two-path transmitter and receiver diversity. The

implemented DICM hardware module is represented in following Fig. 4. One DICM module can process two channels simultaneously for one (A or B) diversity path.

Figure 3. The DPS rack of the RBS system, including the ADCB board.

In the DICM, we used a commercial DAC chip, the AD9777, made by Analog Devices, which converts a digital signal to an analog signal[7]. The chip has x2/x4/x8 interpolation functionality internally and has an output sample speed as high as 400 Msps. In the DICM, the AD9777 operates as high as 256 Msps, which is x4 sampling speed, 64MHz. In addition, we used an off the shelf ADC chip, the AD6645 (Analog Devices), which converts analog signal to digital signal[8]. The AD6645 has a sample speed of 80/105 Msps, and it shows an 89 dBc spurious free dynamic range (SFDR) when the input analog frequency is 70MHz.

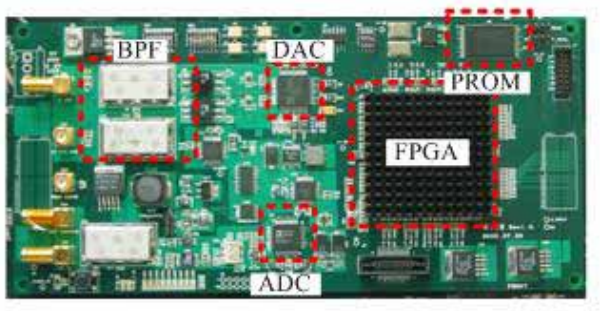

Figure 4. The DICM board Hardware.

The overall digital signal processing for the Digital IF block is implemented with a Field Programmable Gate Array (FPGA) chip, the Vertex II series XC2VP70 (Xilinx Inc.)[9]. This FPGA chip provides interpolation filtering, digital programmable NCO, digital complex quadrature modulation, FA combining for digital upconversion process and FA channelization, demodulation, decimation filtering for downconversion. It also provides a serial communication interface between the ADCB board and the BPB modem board.

3. EXPERIMENTAL RESULTS OF DIGITAL IF TRANSCEIVER

In this section, we examine the experimental results of the presented Digital IF transceiver board. We conducted two tests, a configurability test and a performance test for downlink only. The aim of the configurability test was to identify the reconfigurability to three WiMAX profiles on the same hardware platform using a Reconfigurable Base Station Manager (RBSM) control. The RBSM is a middleware platform that performs reconfiguration, management, and operation of overall RBS systems. The aim of the performance test was to find the variation of performance according to the changes of sampling clock purity. Figure 5 represents the overall test configuration for downlink.

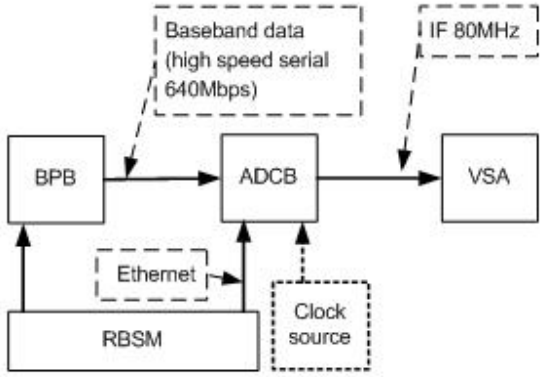

Figure 5. The overall downlink test configuration.

The interface between the BPB and the ADCB is a fabric interface, which is one of the five ATCA backplane interfaces and is implemented by using MGT technology included in FPGAs. The speed of this serial communication is as high as 640 Mbps for a WiMAX downlink transmission. The ADCB upconverts the digital baseband signal from BPB to an IF analog signal of 80 MHz. This signal was measured using Vector Signal Aanlyzer (VSA) equipment commercially available.

To verify the reconfigurability to the three WiMAX profiles according to the RBSM mode change commands,

we measured the spectrum and constellation of each WiMAX profile using the VSA. Measurement results of the three respective WiMAX profiles are presented in order in figs. 6, 7, and 8.

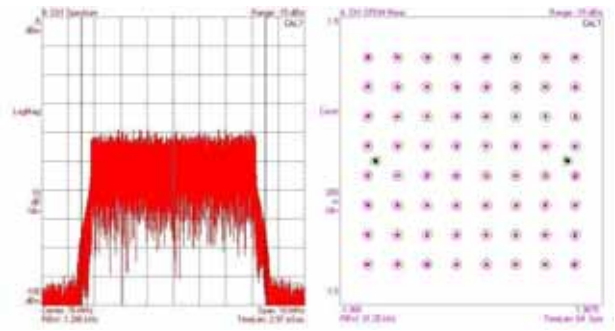

Figure 6. Performance of WiMAX 7 MHz profile (EVM = -43.2 dB).

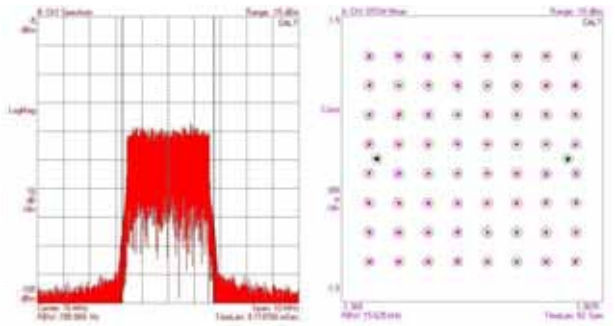

Figure 7. Performance of WiMAX 3.5 MHz profile (EVM = -44.1 dB).

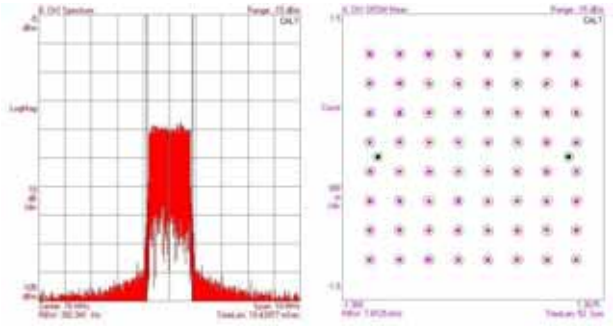

Figure 8. Performance of WiMAX 1.75 MHz profile (EVM = -43.6 dB).

The generated signal at the BPB entering the ADCB through the MGT was a WiMAX OFDM signal having a 5 ms frame duration, a 64 QAM modulated signal, and a code rate of 3/4, with a different signal bandwidth according to each profile. We used the EVM value as a performance criterion in this paper. As can be seen in figs. 6 through 8, the three WiMAX profiles show similar EVM performances. The input sampling clock of the ADCB used to obtain these three test figures was a clock which is Phase Locked Loop (PLL) locked clock to the 10MHz reference clock provided by clock generation and distribution block (CGDB). CGDB board generates and distributes the required clock for overall RBS systems.

In this study, we adopted three sampling clock types that had different phase noises to evaluate the performance degradation of the Digital IF transceiver. The three sampling clock types were designated as follows, according to the measured value of a phase noise at a 10 KHz frequency offset from the selected sampling frequency of 64 MHz: Clock I, with a phase noise of -91.1 dBc/Hz; Clock II, with a phase noise of -112.4 dBc/Hz; and Clock III with a phase noise of -118 dBc/Hz. Clock I was a differential clock received from CGDB through ATCA backplane generated by using a Voltage Controlled Crystal Oscillator (VCXO) on the CGDB board. Clock II was generated by a commercially available function generator. Finally Clock III was a PLL locked clock to the 10MHz reference clock provided by CGDB through an analog cable using a specifically developed PLL module on the ADCB. Clock III had the highest clock purity among the three clock types in terms of phase noise.

We measured the upconverted analog IF output signal of analog 80 MHz with a VSA by changing the input sampling clock source, as represented in Fig. 5. Figure 9 shows an ADCB output performance of a WiMAX 7 MHz profile when using Clock I as a sampling clock source. The EVM performance decreased by 13.7 dB for Clock I as compared with Clock III. Clock I had a higher phase noise than Clock III, about 26.9 dB, as mentioned above.

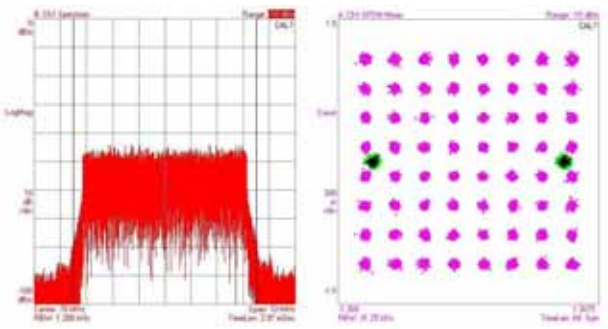

Figure 9. Performance of a WiMAX 7 MHz profile when using Clock I (EVM = -29.5 dB).

The EVM performance of Clock II shown in Fig. 10 reveals a degradation of 0.8 dB compared to Clock III. The phase noise difference between Clock II and Clock III was 5.6 dB. This result indicates that Clock II has a sufficiently low phase noise of -110 dBc/Hz to achieve reasonable performance. For Clock II experimental results revealed a small degradation of EVM performance compared to Clock III when considering the two other WiMAX profiles, which had bandwidths narrower than 7 MHz.

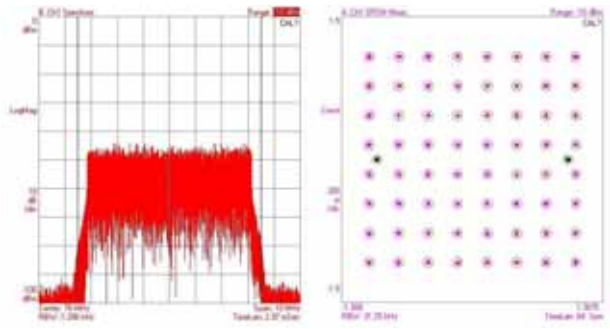

Figure 10. Performance of WiMAX 7 MHz profile when using Clock II (EVM = -42.4 dB).

The EVM performance of each WiMAX profile adopted for the three different sampling clock types are shown in Table 4. The experimental results show that the EVM value of the downlink IF output signal for Clock I decreased by 13 ~ 14 dB more than that of Clock III in the 7 MHz profiles, the result being unrelated to the WiMAX profile that was operating. In addition, it was determined that Clock II, in contrast to Clock III, has sufficiently low sampling clock jitter to deliver high performance with cost-efficiency.

Table 4. EVM performance of each profile for each clock type

Profile / Clock type	7MHz	3.5MHz	1.75MHz
Clock I (dB)	-29.5	29.6	-30.6
Clock II (dB)	-42.4	-43.8	-42.6
Clock III (dB)	-43.2	-44.1	-43.6

4. CONCLUSIONS

In this paper, we have verified that the implementation of a reconfigurable Digital IF transceiver that can support three WiMAX profiles using SDR technologies by examining the spectrum and the constellation on IF output through off-the-shelf equipment. In addition, experimental results have shown that the EVM value of the downlink IF output signal for a clock with a relatively high phase noise decreased by more than 13 dB as compared to a good quality clock, the result being unrelated to the WiMAX profile that was operating.

5. REFERENCES

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