

RE-CONFIGURATION TECHNIQUES FOR SDR ARCHITECTURES

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ABSTRACT

Concepts and techniques for re-configurability in mobile wireless terminals are presented which can be used in future SDR terminals. The techniques are used to obtain a multi-mode operation, so that a mobile terminal can support different wireless standards with the same hardware platform. This is demonstrated first by using UMTS and its extension as well as GSM. The work is concentrating on the physical layer where RF front-end and baseband are covered

1. INTRODUCTION

Future mobile terminals need to support various wireless standards. At the same time the complexity and size of the mobile terminal should not increase, since cost and power consumption need to be kept at a minimum. This is particular important in order to obtain a later market acceptance. The IST funded project MuMoR (Multi-Mode Radio) has its main objectives in investigating mobile terminal architectures for multi-mode operation. The investigated radio systems are mainly UMTS/FDD, UMTS/TDD, and HSDPA/FDD. Additional investigations towards the operability with other cellular and non-cellular standards like GSM and WLAN (IEEE 802.11 a/b) are also considered. MuMoR covers physical layer aspects for the analogue RF part as well as for the digital baseband part of a terminal. Because of investigating the analogue and digital parts of the system in only one project, particular attention will be on the simulation of the overall transceiver system and the definition and design of the interface circuits, like the ADC. In order to minimize the hardware complexity for a multi mode transceiver re-configurable techniques in the front-end and baseband part of the project are applied. Section 2 of this abstract presents the research areas and results in the radio frequency front-end domain, whereas section 3 focuses on investigations concerning digital baseband.

2. RADIO FREQUENCY FRONT-END

2.1. Multi Mode Front-End Architecture

The Direct Conversion Receiver (DCR) uses only lowpass filters in the analogue baseband part. This kind of filter is easier to change in term of its bandwidth. Research on the DCR architecture has shown that this topology is well suitable for RF system integration [3][4]. In Figure 1 the architecture of a DCR used in the project MuMoR is shown. The analogue baseband filters have a 5th order Butterworth characteristic that is distributed over several filter stages. The specifications of the filters have a flexible bandwidth, so that they are re-configurable between 2.3 MHz and 200 kHz [5].

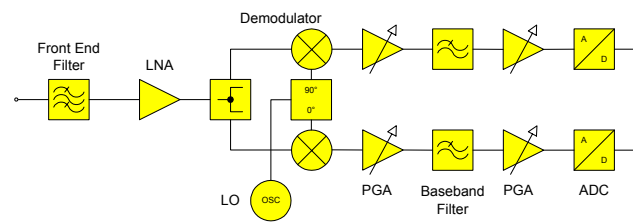


Figure 1 – Direct Conversion Receiver Architecture

Not only the analogue baseband filters need to be re-configurable, but also the frequency synthesis or the interfaces between the analogue and digital part need this re-configuration technique in order to support multi mode operation.

2.2. Techniques for Re-configurability

Beside the work on the architecture level for multi mode operation there is a need to have techniques, which allow the front-end to switch between different modes. In terms of RF re-configurability that means mainly switching between different paths, setting of gain or bandwidth or the selection of the right resonator tank. This is applied on the circuit and baseband level.

A component, which is able to support that kind of functionality, is MEMS (Micro Electro Mechanical Systems).

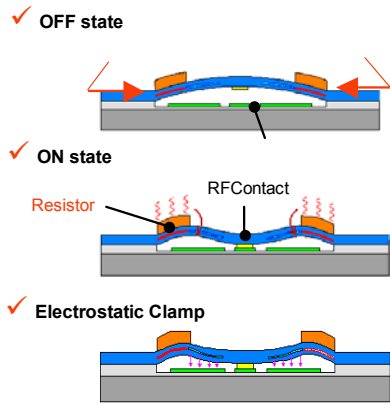


Figure 2 – MEMS used as a switch

In MuMoR this component are investigated in terms of its capability to support multi mode operation in the RF front-end. First results demonstrate that the use of these components at some point in the front-end is possible e.g. switch between GSM and UMTS frequency bands [3]. In figure 3 a MEMS component, which is used as a switch, is shown. This MEMS switch has an insertion loss of 0.3 dB and an isolation of more than 50 dB at a frequency of 2 GHz [4]. The actuation voltage is low as 2V. Hence the MEMS switch shows a big potential to be used in mobile terminals.

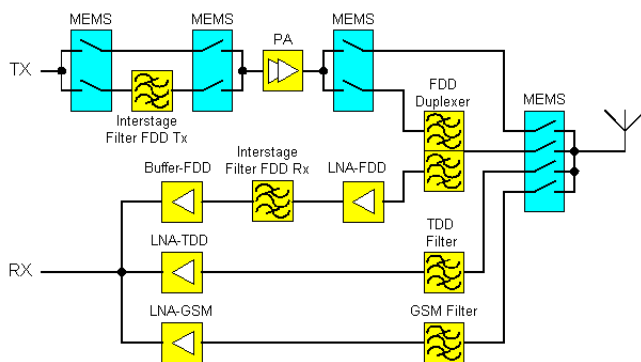


Figure 3 – Front-End module of a Multi Mode Terminal

Figure 3 shows the proposed architecture of a re-configurable RF front-end module investigated in MuMoR. The design presented here is supporting UMTS FDD, TDD mode and the GSM mode.

2.2. Re-configurable RF Components

The voltage controlled oscillator (VCO) is a key component in every synthesizer and therefore an important component to generate different frequencies. Hence, it is a central element for multi mode radios. In figure 4 a multi mode VCO is depicted. One objective is that the VCO can be used for RX and TX that is possible for the UMTS/TDD mode and for GSM. The different frequencies are generated by changing the resonator tank of the VCO digitally with MOS transistors, so called Switched Capacitor Array (SCA). Because of the DCR architecture and in order to reduce LO to RF coupling, the output frequency is up to 5 GHz.

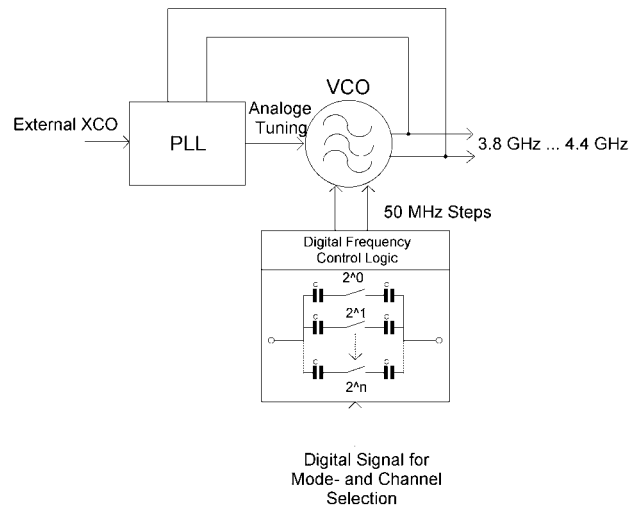


Figure 4 – Multi Mode Voltage Controlled Oscillator

The most severe requirement on the spectral purity of the VCO is that the phase noise has to be smaller than -145 dBc/Hz at 20 MHz offset, which is when the radio is in transmit mode. The current consumption is as low as 4 mW. The VCO has been implemented in an advanced SiGe - BiCMOS technology (70 GHz/0.25um).

To use the same baseband receive chain for different modes the baseband filters need to be re-configurable as well. Beside a high linearity and low power design the bandwidth and gain need to be set for multi mode operation. In Figure 5 the frequency response of an analogue baseband filter is shown which has also been implemented in an silicon semiconductor technology. The filter topology is based on a gm-C filter design. This filters covers in its actual version UMTS and GSM and could be extended towards higher bandwidth which are required in WLAN systems.

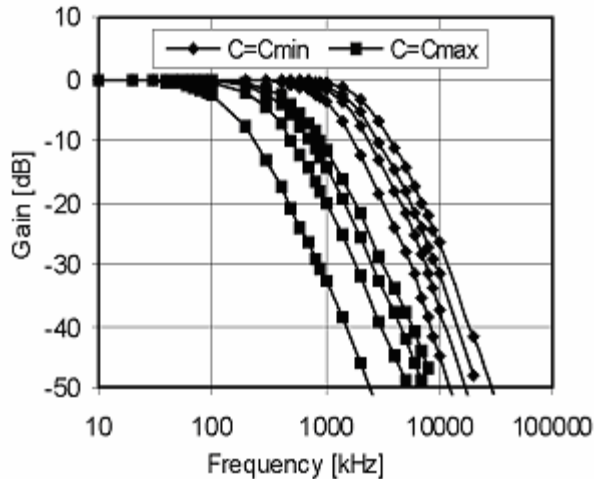


Figure 5 – Implemented Analogue Baseband Frequency Response

3. DIGITAL BASEBAND

3.1. Needs for Re-configurability in the digital baseband

Mobile terminals for 3G, 3G+ and 4G telecommunication systems require an increasing amount of high-speed signal processing in the digital baseband. This demand is caused by the selection of algorithms, which have to be implemented to achieve a required performance. The traditional design alternatives, hardwired ASICs and SW on digital signal processor are no longer feasible for multi-mode systems operating in a high data rate regime. A pure SW solution on processors would well support the multi-mode design, but often is too slow or inefficient. A pure HW solution on the is not flexible enough to take advantage of the similarities of the different systems and requires the parallel implementation of all these systems, which is not efficient.

A system that either operates in FDD using UMTS and HSDPA channels or in TDD using UMTS channels only is examined here. These two similar systems operate mutual exclusive in time offers some potential for re-configuration and enables resource sharing on the implementation level, leading to a more area-efficient design. However, optimization in terms of area is only one issue, having an eye on the power consumption is often even more important.

3.1.1. Re-configuration by Algorithm Selection

There are some measures to be considered during the definition of the applied algorithms to favor the implementation. This is similar to a power optimization process, which also has to be applied at all levels of abstraction in the planning and design to reach an optimum.

A key issue for the selection of algorithms to favor the re-configurability is to identify those using the same kind of fundamental operations or common set of operations. During the conception of a *single-mode* system there is only a trade-off between performance and implementation effort whereas in a *multi-mode* system this optimization becomes a multi-dimensional problem due to its effect on the performance on all modes to be supported.

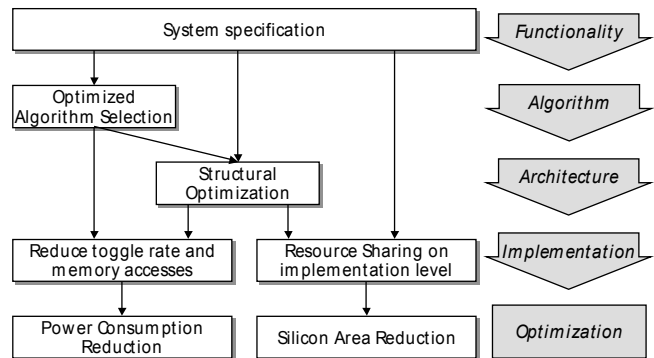


Figure 6 – (Multi-mode) Design Optimizations

Figure 6 shows how the system specifications can either directly offer potentials for e.g. resource sharing inherently. Furthermore, the combination of a clever algorithm selection with a structural optimization, i.e. the addition of means on architectural level, will also offer potentials for resource sharing reducing the silicon area either by removing registers and combinational logic or by reducing the amount of memory required.

We started with optimal algorithm solutions for the distinct modes FDD and TDD. For the channel estimator (CE) this meant using a correlator based CE operating on the Common Pilot Channel and Rake receiver for FDD as well as a DFT based CE (Steiner Algorithm [8]) operating on the midamble with Joint Detection for TDD. For single-mode system these both solutions are doing well but for a FDD/TDD multi-mode system a more optimal solution is required. After modifying the algorithm selection towards a *common* optimum a certain loss in performance and/or increase in computational complexity may occur but the benefit for the final implementation can still prevail.

The Steiner algorithm has been replaced by a correlator based one as used in FDD. In this way, the FDD solution is not affected at all, which makes it easier to determine the “cost” of the optimization. Simulations showed that the computational complexity increase for TDD to achieve similar performance for the test cases defined by 3GPP, e.g. “DL reference measurement channel (2 Mbps), 3.84 Mcps TDD Option” according to chapter A.2.8.1 of [9]. The obvious benefit is the re-use of HW components for both modes. There is no need to additionally implement an FFT structure any more.

For components that will be implemented in SW it is much more difficult to express the gain in such case. However there are cases, where it is still apparent, e.g. when the DSP has special support for certain algorithms, these ones should be used preferably. Examples are shown in the next sections.

3.1.2. Implementation Level Optimizations

The results of any optimization will be seen on implementation level. Finally, the architecture and the implementation have to support the optimizations, which have been made on algorithm level. For multi-mode design a higher degree of flexibility has to be achieved, namely more flexible than dedicated HW but with competing performance, i.e. re-configurable or soft-configurable. There have been several approaches developed to achieve a soft-configurable design. There are three main categories:

I. Monolithic microprocessor with extensions

Here the proposals are focused on a general-purpose microprocessor, very similar to other well-known microprocessors or DSPs, and the design-flow for control-oriented programming is very similar to application development on DSP platforms. The main differences are the extensions of ASIC-like parts within the microprocessor to speed up certain operations so that the high processing power demands of telecommunication applications can be met. The biggest problem in this approach is the bottleneck of data throughput because all data mostly has to be transferred via the processor bus. (Example: [10]).

II. FPGA-like structure with big number of low complexity processing elements

Other approaches are similar to FPGA-like structure with a symmetrical matrix interconnection network, consisting of many low-complexity processing elements, mostly identical, to solve distinguished computation problems. The speed-up is mainly achieved by massive parallel processing. Algorithms are divided into very basic operations not more complex than additions or multiplications. Here the significant problem lies in the great challenges of the compiler to keep all processing elements busy in operation to maximize the efficiency. (Example: [11])

III. Multiprocessor concepts

The last category is based on a multiprocessor approach, defined by a network of complex general-purpose processors, similar to already available cores connected by a processor bus or communicate via shared memory. The design flow is very similar to developing applications on single-processor systems for parallelizable algorithms, but as more communication between parallel computed algorithms is needed the effort of synchronization and scheduling becomes more and more obvious to the designer.

A problem that can occur in this approach is the bottleneck of data throughput on the shared processor bus. (Example: [12])

We selected an implementation, fitting best to the first category. To achieve highest flexibility it is microprocessor-centric with acceleration extensions for selected operations. In section IV an example for a useful extension to a DSP for the investigated enhanced 3G scenario is given.

All previous methods were focused on optimization of computational parts of the design, the combinational logic and registers. But there is a second domain that has to be covered by the implementation independent of the HW/SW partitioning: The storage of (intermediate) data. When a system is operating in different modes one can imagine that the amount of data to be stored varies. If the HW architecture allows the usage of centralized shared memories which several modules can access, the required *total* memory for the system is ideally as big as the memory requirements of the operating mode with the *biggest* memory consumption, i.e.

$$mem_{total} = \text{MAX}(mem_{mode 1}, mem_{mode 2}, \dots, mem_{mode n}).$$

The investigated scenario offers some potential to share memory. The Cell Searcher (CS) memory requirements depend on the operating modes FDD and TDD. The front-end of the CS as depicted in Figure 7 mainly consists of two parts, P-SCH matched filter and S-SCH correlator. Arithmetic of P-SCH computation in FDD and TDD is similar, but TDD requires more memory. Taking into account that during FDD operation also the High-Speed channel may be active there is usage for the additional memory: The H-ARQ buffer between the two stages of the rate matcher. Depending on the UE category the number of soft bits available in the virtual IR buffer (N_{IR}) may have a size of up to 28.800 soft bits. [13]

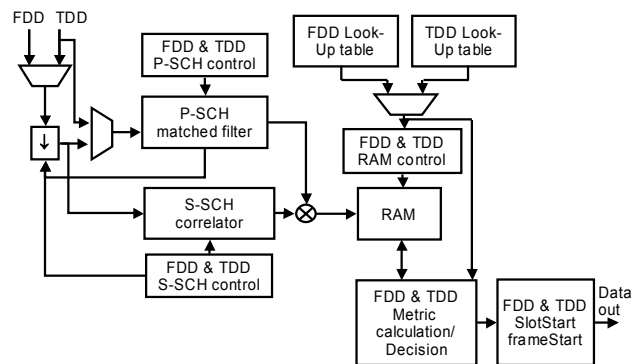


Figure 7 – FDD/TDD Cell Searcher

IV. Re-configurability through DSP co-processing

The most flexible approach is the ideal software radio, performing all computations in one or more DSPs.

However, in physical layer of radio communication systems there are typically algorithms operating on bit-level, which could be done on a DSP but are very inefficient because normal DSPs allow only operation on bigger data structures. Also register and memory accesses do not allow bit-level operations. In the UMTS/HSDPA physical layer the following operation can be counted to this class:

- CRC Encoder / Decoder (used in all modes)
- Turbo Encoder (used in all modes)
- Convolutional Encoder (used in FDD and TDD modes)
- Bit Scrambler / DeScrambler (used in TDD mode)

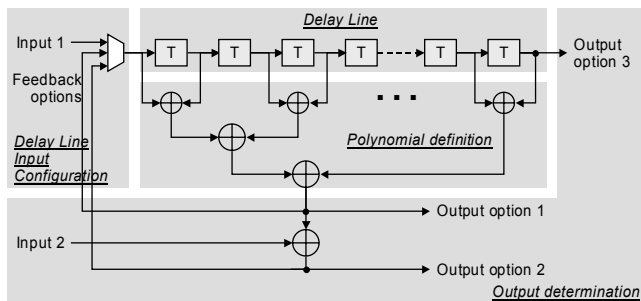


Figure 8 – Abstract universal bit level arithmetic unit

Figure 8 shows an universal bit level arithmetic unit which can fulfill all the operations listed above, which are all based on bit pipeline, bit shift registers or filter structures with XOR operations on different stages of the pipeline. Several kinds of configurations are possible, i.e. for input signal, output signal, polynomial definition and length of the delay line. For example the filter output can be used directly as output data stream (Output option 1 in above figure) or further operations to be done with this data stream, e.g. add an input sequence on it (Output option 2). To further optimize of this bit level arithmetic unit a dedicated memory adapter is useful to map the words from the memory into single bits and vice versa. A compressing unit is required that uses all bits of a memory word by storing neighboring bits into one standard memory word. With this approach the required amount of standard memory words is reduced. To reduce the number of memory accesses cache is required mapping the memory words to a bit level memory. This includes the typical cache functionality like writing back after modifications and also requires some kind of address decoding as depicted in Figure 9. The bit-level cache is being addressed with a bit-level address. Bit level operations are typically on successive bits, burst read and write access should be available. Standard memory access, which the cache has to perform in case of write back (write access) and cache miss (read access), has to be handled by an address mapper containing e.g. a look-up table (LUT) to generate the standard memory address out of the bit-level address.

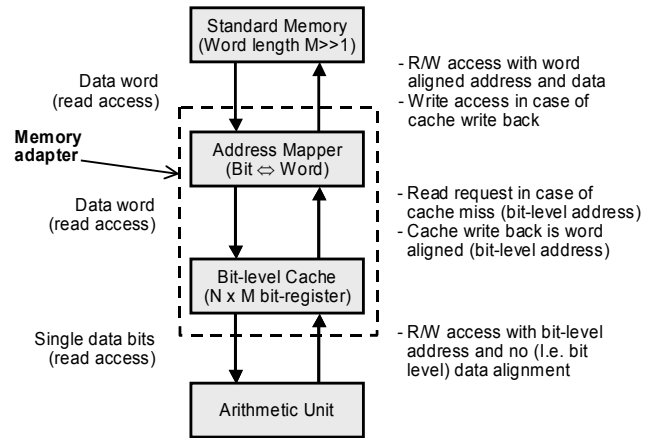


Figure 9 – Bit-to-Word Memory Adapter

The advantage of combining the flexible bit level arithmetic unit with the presented memory adapter is that the number of memory adapters can be reduced because the attached arithmetic unit does process several different algorithms, thus only few of them are required, depending on HW performance and system demands. [14]

4. CONCLUSION

Various techniques for re-configurability of RF front-ends as well as digital baseband have been presented, which can be used in SDR mobile terminals. A flexible and well know architecture for the front-end has been chosen and combined with circuits and RF components, which can be re-configured to different wireless standards. Several goals have been considered for the digital baseband approach in order to achieve an optimum solution that meets the requirements of the communication systems as well as commercial aspects. The chosen technical approach shows due to the right combination of system architecture, circuits and components, a re-configurability radio can be designed to meet future mobile terminal requirements supporting all different standards.

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